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LIGHT MANAGEMENT BY PHOTOCHEMICALLY ETCHED INVERTED STRUCTURES FOR SILICON SOLAR CELLS

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Approval of the Graduate School of Natural and Applied Sciences, Atılım University.

Assoc. Prof. Dr. Gökhan TUNÇ
Director

I certify that this thesis satisfies all the requirements as a thesis for the degree of **Master of Science in Electrical and Electronics Engineering, Atılım University**.

Prof. Dr. Reşat Özgür DORUK
Head of Department

This is to certify that we have read the thesis LIGHT MANAGEMENT BY PHOTOCHEMICALLY ETCHED INVERTED STRUCTURES FOR SILICON SOLAR CELLS submitted by GÜNTUĞ VURAL and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

Prof. Dr. Alpan BEK
Co-Supervisor

Prof. Dr. Reşat Özgür DORUK
Supervisor

Examining Committee Members:

Prof. Dr. Ahmet BİNGÜL
Department of Engineering Physics,
Gaziantep University

Prof. Dr. Reşat Özgür DORUK
Department of Electrical and Electronics Eng.,
Atılım University

Doç. Dr. Özge SÜRÜCÜ
Department of Electrical and Electronics Eng.,
Atılım University

Date: *June 30, 2025*

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Name, Last Name : GÜNTUĞ VURAL

Signature :

ABSTRACT

LIGHT MANAGEMENT BY PHOTOCHEMICALLY ETCHED INVERTED STRUCTURES FOR SILICON SOLAR CELLS

Vural, Güntuğ

M.S., Department of Electrical and Electronics Engineering

Supervisor : Prof. Dr. Reşat Özgür DORUK

Co-Supervisor : Prof. Dr. Alpan BEK

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While crystalline silicon solar cells currently dominate the photovoltaic market, improving their efficiency through advanced surface texturing remains a significant research challenge. This study introduces an innovative single-step inverted nanohole surface texturing approach using in-situ photochemical etching (PCE) on n-type silicon solar cells, employing a continuous-wave laser (532 nm) in an HF/H_2O_2 aqueous solution. Compared to conventional texturing techniques, the nanostructures produced via PCE have been shown to be deeper, denser, and more effective across a broad spectral range. Scanning electron microscopy (SEM) images confirmed the formation of inverted nanohole structures with random distribution and non-uniform morphology across the silicon surface. Photon trapping was significantly enhanced, as evidenced by reduced average reflectance, down to 17.5 percent for saw damaged (SD) and 22.5 percent for saw damage removed (SDR) wafers, across the 300–1200 nm wavelength range, along with increased haze resulting from enhanced light scattering. Furthermore, simultaneous photochemical etching demonstrated distinct advantages over conventional sequential methods, including continuous oxide removal, deeper structures, and improved profile anisotropy suitable for micro-electromechanical

systems (MEMS) fabrication. Notably, the proposed method (SS-INH-PCE) inherently eliminates the need for a separate saw damage removal step, simplifying the process and reducing overall chemical and thermal loads. The simplicity, reproducibility, and optical efficiency of the SS-INH-PCE process highlight its potential for scalable industrial integration, positioning inverted nanohole texturing as a promising pathway for next-generation high-efficiency solar cells and MEMS technologies.

Keywords: Crystalline Silicon, Single-Step Inverted Nanohole, Laser Assisted Etching, Photochemical Etching, Surface Texturing

ÖZ

SİLİKON GÜNEŞ HÜCRELERİ İÇİN FOTOKİMYASAL OLARAK KAZINMIŞ TERS YAPILARLA IŞIK YÖNETİMİ

Vural, Güntuğ

Yüksek Lisans, Elektrik ve Elektronik Mühendisliği

Tez Yöneticisi : Prof. Dr. Reşat Özgür DORUK

Ortak Tez Yöneticisi : Prof. Dr. Alpan BEK

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Kristal silisyum güneş hücreleri günümüzde fotovoltaik pazara hâkim olsa da gelişmiş yüzey desenleme teknikleriyle verimliliklerinin artırılması hâlâ önemli bir araştırma zorluğu olarak öne çıkmaktadır. Bu çalışma, n-tipi silisyum güneş hücreleri üzerinde sürekli dalga modunda çalışan bir lazer (532 nm) ve HF/H_2O_2 sulu çözeltisi kullanılarak uygulanan yerinde (in-situ) fotokimyasal aşındırma (PCE) yöntemiyle gerçek-leştirilen yenilikçi bir tek adımlı ters nanodelik yüzey desenleme yaklaşımını tanıtmak-tadır. Geleneksel desenleme teknikleriyle karşılaştırıldığında, PCE yoluyla üretilen nanoyapıların daha derin, daha yoğun ve geniş bir spektral aralıkta daha etkili olduğu gösterilmiştir. Taramalı elektron mikroskobu (SEM) görüntüleri, silisyum yüzeyinde rastgele dağılmış ve düzgün olmayan morfolojiye sahip ters nanodelik yapılarının oluşumunu doğrulamıştır. 300–1200 nm dalga boyu aralığında, test edilen test örnek-lerinde ortalama yansıtma değerlerinin testere hasarlı (SD) yüzeylerde %17.5'e ve testere hasarı giderilmiş (SDR) yüzeylerde %22.5'e kadar düşmesi ve artan ışık saçılma-sına bağlı olarak yükselen haze değerleri, foton tuzaklamada kayda değer bir iyileşme olduğunu göstermiştir.

Ayrıca, eşzamanlı fotokimyasal aşındırma yöntemi, sürekli oksit giderimi, daha derin

yapılar ve mikro-elektromekanik sistemler (MEMS) üretimi için uygun geliştirilmiş profil anizotropisi gibi geleneksel ardışık yöntemlere kıyasla belirgin avantajlar sergile-miştir. Özellikle önerilen yöntem (SS-INH-PCE), ayrı bir testere hasarı giderme adımına duyulan ihtiyacı ortadan kaldırarak süreci sadeleştirmekte ve toplam kimyasal ile termal yükü azaltmaktadır. SS-INH-PCE sürecinin sadeliği, tekrarlanabilirliği ve optik verimliliği, bu yöntemin sanayi ölçeğinde uygulanabilirliğini ön plana çıkarmakta; ters nanodelik desenlemesini ise yeni nesil yüksek verimli güneş hücreleri ve MEMS teknolojileri için umut verici bir yol olarak konumlandırmaktadır.

Anahtar Kelimeler: Kristal Silisyum, Tek Adımlı Ters Nanodelik, Lazer Destekli Aşındırma, Fotokimyasal Aşındırma, Yüzey İşlemesi

To My Family

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LIST OF SYMBOLS AND ABBREVIATIONS

SS-INH-PCE	:	Single-Step Inverted Nanohole Photochemical Etching
SD	:	Saw-Damaged
SDR	:	Saw-Damage-Removed / Removal
c-Si	:	Crystalline Silicon
PV	:	Photovoltaic
PCE	:	Photochemical Etching
SEM	:	Scanning Electron Microscope / Microscopy
IR	:	Infrared
CW	:	Continuous-Wave (Laser)
HF	:	Hydrofluoric Acid
H_2O_2	:	Hydrogen Peroxide
DI	:	Deionized (Water)
MEMS	:	Microelectromechanical Systems
PERL	:	Passivated Emitter and Rear Locally-Diffused
FWHM	:	Full Width at Half Maximum
RCA	:	Radio Corporation of America (standard wafer cleaning)
n-type	:	Electron Majority Carrier Silicon
AR	:	Anti-Reflective
PECVD	:	Plasma-Enhanced Chemical Vapor Deposition
EHT	:	Electron High Tension (SEM voltage)

FF	:	Fill Factor
WD	:	Working Distance (in SEM)
SE2	:	Secondary Electron Detector (type 2)
μ-PCD	:	Microwave Photoconductive Decay
QSSPC	:	Quasi-Steady-State Photoconductance
p-type	:	Hole Majority Carrier Silicon
MIS	:	Metal-Insulator-Semiconductor
λ	:	Wavelength (in nm)
R	:	Reflectance (in %)
H	:	Haze (in %)
P	:	Laser Power (in W)
d	:	Diameter (spot or nanohole)
L	:	Nanohole Depth or Etch Length
n	:	Refractive Index
θ	:	Angle of Incidence
E	:	Electric Field Intensity
t	:	Etching Time (in s or min)
A	:	Area (typically in cm^2)
D	:	Beam Diameter (in mm or cm)
I	:	Irradiance (in W/cm^2)

CHAPTER 1
INTRODUCTION

In this thesis, a single-step laser-assisted photochemical etching (SS-INH-PCE) method is developed to fabricate inverted nanohole structures on crystalline silicon (c-Si) wafers for broadband light-trapping applications. This approach utilizes a continuous-wave (CW) 532 nm laser focused onto the silicon surface immersed in an HF/H_2O_2/DI water solution, allowing for localized and maskless texturing of the wafer. The proposed method offers simultaneous surface texturing and saw-damage removal, thereby simplifying the conventional multi-step process used in high-efficiency solar cell fabrication.

Nanostructured surfaces such as inverted pyramids and nanohole arrays are widely investigated due to their superior light-trapping capabilities and compatibility with planar device designs. However, existing nanofabrication methods, such as reactive ion etching and lithography-based patterning, are often limited by high cost, complexity, and scalability challenges [1]. The SS-INH-PCE method aims to overcome these limitations by providing a low-damage, lithography-free solution that enables high-density nanostructure formation over large areas with minimal thermal budget.

The experimental strategy involves applying the SS-INH-PCE method to three different wafer types: saw-damaged (SD), saw-damage-removed (SDR), and standard untreated wafers. Reflectance and haze measurements are used to assess the optical performance of the treated surfaces, while SEM imaging provides insight into the morphological characteristics of the nanostructures. The results indicate that the process is capable of significantly reducing reflectivity, yielding average values of 17.5% for SD and 22.5% for SDR wafers, across the 300–1200 nm spectral range, with a corresponding increase in haze due to enhanced scattering effects.

This study illustrates that the SS-INH-PCE technique integrates optical surface texturing and defect reduction into one simplified process, providing an efficient

and scalable approach for silicon photovoltaics. Its gentle etching characteristics and adaptability also indicate potential applicability to other optoelectronic devices, such as thin-film solar cells.

1.1 Background and Research Motivation

For many years, crystalline silicon solar cells have remained fundamental to photovoltaic technologies, largely owing to their proven reliability, mature manufacturing processes, and notably high energy conversion efficiencies [2]. However, the theoretical Shockley–Queisser limit of single-junction c-Si solar cells (33.7%) imposes an upper bound that necessitates novel light-trapping schemes to approach practical maximum efficiency [3].

Surface texturing methods that increase light path length and reduce front surface reflectivity have proven to be effective tools to surpass traditional efficiency plateaus. Conventional pyramid-based textures and random features achieved through anisotropic etching, while effective, are often insufficient when targeting nanophotonic effects or when applied to thinner wafers [4].

In this context, nanostructuring techniques have garnered significant interest. Inverted nanohole structures, in particular, enable enhanced light trapping via diffraction and resonant scattering mechanisms, offering broadband anti-reflective behavior. Yet, their fabrication usually requires complex lithographic steps or high-cost equipment, limiting large-scale implementation [5].

In this study, the SS-INH-PCE method was developed to overcome existing limitations by providing a simpler, scalable, and chemically efficient approach for producing inverted nanostructures. Additionally, saw damage is inherently removed during the etching process, eliminating the need for an additional surface damage removal step. Through this dual functionality, the overall fabrication process is simplified, chemical usage is reduced, processing time is shortened, and thermal requirements are decreased, which are factors crucial for industrial feasibility.

1.2 Outline of the Thesis

Chapter 2 provides the theoretical background and outlines the research motivation. It discusses the current challenges in photovoltaic technologies, particularly the limitations of conventional surface texturing methods, and introduces the concept of photochemical etching with an emphasis on its potential for nanostructure fabrication on silicon surfaces.

Chapter 3 describes the materials and experimental methods employed in this study. It presents the detailed configuration of the optical setup, the preparation of the chemical solution, and the implementation of the SS-INH-PCE technique. The measurement procedures and characterization tools used to evaluate surface morphology and optical performance are also explained. The chapter concludes with a discussion on potential future directions, with particular emphasis on adapting the SS-INH-PCE method for full-wafer processing and its integration into photovoltaic device manufacturing.

In Chapter 4, the primary outcomes of this research are summarized. The advantages of the SS-INH-PCE method are discussed, highlighting its capability to enhance light trapping and processing efficiency, as well as its potential to contribute to the advancement of high-efficiency photovoltaic technologies.

CHAPTER 2
SILICON SOLAR CELL TECHNOLOGY

2.3 Silicon Wafer Fabrication Techniques

Silicon wafers are critical components of semiconductor technology, including solar cell fabrication. These wafers are prepared for high-performance applications using precise structural, electrical, and optical preparations. Among these techniques, wafer slicing, saw damage introduction, and subsequent saw damage removal are key stages impacting the overall quality and performance of the final devices [6].

2.3.1 Silicon Wafer Production Methods

Silicon wafers are primarily produced through two distinct crystallization methods: the Czochralski (CZ) growth method and the Float Zone (FZ) method. Both processes start with highly pure polycrystalline silicon and yield high-purity monocrystalline silicon, but their approaches and outcomes differ [7].

In the Czochralski method, polycrystalline silicon is melted in a quartz crucible. A seed crystal is then dipped into the molten silicon and slowly withdrawn while rotating, causing silicon to crystallize at the interface. This method is widely utilized as it can produce large-scale silicon ingots. However, impurities from the crucible material, especially oxygen, can introduce defects and contamination of the silicon structure [7].

Conversely, in the float zone method, a molten Zone is moved vertically along a polycrystalline silicon rod. A seed crystal initiates the crystallization process, and by carefully controlling temperature gradients and pulling speeds, it is possible to produce silicon crystals with extremely high purity and minimal defects. Such a method avoids crucible-related impurities, which creates an advantage for applications requiring excellent electrical and structural integrity, such as high-performance photovoltaic

devices and electronic components [7,8].

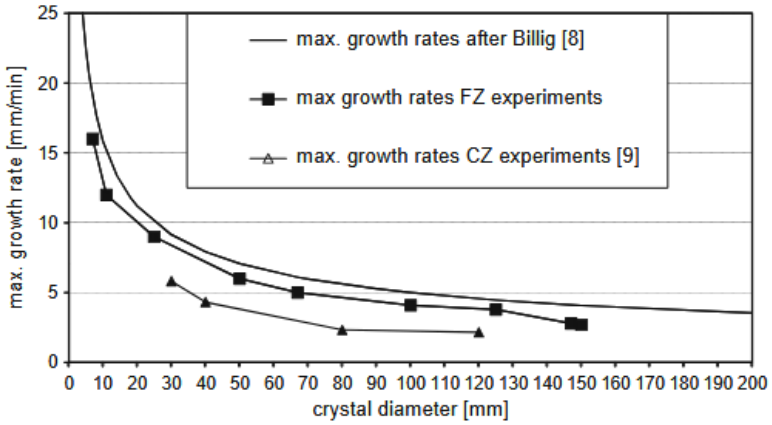


Figure 2.1 Maximum growth rates: Calculated after Billig [8], from FZ experiments at the ICG Berlin and CZ experiments [7].

2.3.2 Wafer Slicing and Saw Damage

Large cylindrical silicon ingots are sliced into thin wafers following crystal growth. This procedure is usually performed with diamond-coated inner diameter (ID) saws or wire saws. The slicing process plays a significant role in the mechanical and surface properties of the wafer. This mechanical process produces defects and microstructural damage on the wafer surfaces, which is commonly called ”saw damage” [9].

Saw damage encompasses all the structural defects created during wafer slicing, including microcracks, crystal dislocations, residual stresses, and surface roughness. The depth and severity of saw damage depend significantly on the slicing method and parameters, such as saw blade or wire tension, abrasive particle size, cutting speed, and cooling conditions. Typically, saw damage is observed within a depth ranging from a few micrometers to tens of micrometers from the wafer surface [10]. This damaged layer is detrimental to device fabrication for multiple reasons:

- **Mechanical Weakness:** The presence of microcracks reduces wafer strength and increases susceptibility to breakage during subsequent handling or processing [10].
- **Electrical Performance:** Defects and crystal dislocations serve as

recombination centers and significantly decrease minority carrier lifetimes, an extremely significant parameter for photovoltaic and electronic applications [10].

- **Surface Roughness:** High roughness prevents uniformity and reliability of subsequent surface processing steps, such as photolithography or metal deposition [10].

2.3.3 Saw Damage Removal Techniques

Given the detrimental effects of saw damage on silicon wafer production, a follow-up step of removal of this damaged layer is called saw damage removal. A few techniques are developed and refined for this purpose, selected among others, according to cost-effectiveness, throughput, and wafer application requirements:

2.3.3.1 Mechanical Polishing

Mechanical polishing, or lapping, is a traditional and extensively used method to eliminate saw damage. It employs abrasive particles suspended in a slurry to grind the wafer surfaces mechanically. The damaged layer is progressively removed through successive polishing steps with decreasing abrasive particle size, yielding smoother and defect-reduced surfaces. However, this method can lead to surface degradation, often making additional chemical polishing necessary to achieve the desired surface quality [11].

2.3.3.2 Etching

Etching is a material removal process extensively utilized in semiconductor and microfabrication industries to selectively remove layers of material and define intricate patterns, features, or structures on a substrate's surface [12]. In the field of silicon-based devices, etching enables the creation of precise three-dimensional geometries and fine structures that are critical to the functionality and performance of integrated circuits, microelectromechanical systems, and photonic devices[13]. Highly accurate and

reproducible etched features can be created by judiciously controlling parameters such as etchant composition, reaction duration, temperature, and mask design [14].

The etching of a silicon wafer typically begins with applying a patterned mask, which is often composed of photoresist or a hard mask material such as SiO_2 or Si_3N_4. This mask delineates the areas intended for removal. After creating the pattern through lithographic processes, the wafer is treated with the selected etchant, which can be either a liquid solution (wet etching) or a gas/plasma mixture (dry etching). During this step, the etchant removes silicon only from the exposed regions, leaving the masked portions unchanged [15].

Selecting the suitable etchant composition along with the processing parameters yield anisotropic or isotropic etch profiles, allowing structures with specific shapes, depths and defined sidewalls. This degree of precision is significant in MEMS fabrication, where the functionality and reliability of the devices are contingent upon maintaining accurate dimensions and robust structural integrity in the etched features [16].

Thin-film and bulk substrate etching represent key steps in Very Large Scale Integration (VLSI) and micro/nanofabrication processes. Conductive and dielectric thin films (often used as passivation or masking layers) must be selectively removed within VLSI at specific stages of device manufacturing. In micro/nanofabrication, etching encompasses not only thin films but also portions of the underlying substrate (e.g., silicon, glass, or GaAs) to create mechanical micro and nanostructures, such as beams and plates that are essential for device functionality [17].

Two critical factors that determine the effectiveness and outcome of etching operations are selectivity and directionality. Selectivity refers to the etchant's ability to distinguish between the target material and the masking layer, ensuring that only the intended portion of the substrate is removed [17].

Particular material selectivity has become a challenge since plasma etching has entered semiconductor manufacturing. Selectivity encompasses the fundamental need to accurately transfer a specified pattern into the target material while minimizing removing other components, such as the mask or the underlying substrate [18]. Conventionally, selectivity is quantified as the ratio of the etch rate of the desired layer to that of the layer intended to remain intact. Various processes have been developed to fine-tune selectivity for pairs such as SiO_2-to-Si, SiO_2-to-SiN_x, or SiO_2-to-photomask, thereby ensuring effective pattern transfer into the substrate[19]. In general, maintaining etch selectivity is achieved by promoting the formation of an etch-inhibiting film on surfaces not meant to be etched, eventually reducing their etch rate to zero or ”etch stop.” Nonetheless, a certain amount of material is inevitably removed from these protected surfaces prior to reaching the complete etch-stop condition [18].

Directionality pertains to the shape and uniformity of the etched profile. While isotropic etching removes material at a similar rate in all directions, anisotropic etching is sensitive to crystallographic orientations and can yield straight sidewalls or other well-defined structures. Additionally, etching methods can be categorized as wet (liquid-phase) or dry (plasma-based), with different process control, throughput, and compatibility advantages [17].

Dry Etching

The dry etching offers distinct advantages over wet etching. Among these benefits are reduced undercut (facilitating the patterning of narrower lines) and enhanced anisotropy, enabling high-aspect-ratio vertical structure creation [17, 20]. However, dry etching techniques tend to have lower selectivity compared to wet etching, which makes it important to account for the limited resistance of masking materials during the process. Three primary dry etching techniques, high-pressure plasma etching, reactive-ion etching (RIE), and ion milling, each utilize distinct mechanisms to achieve precise directional control during material removal. A key distinguishing factor among these various etching technologies is the process pressure maintained within the etch chamber during the etching operation [17,21].

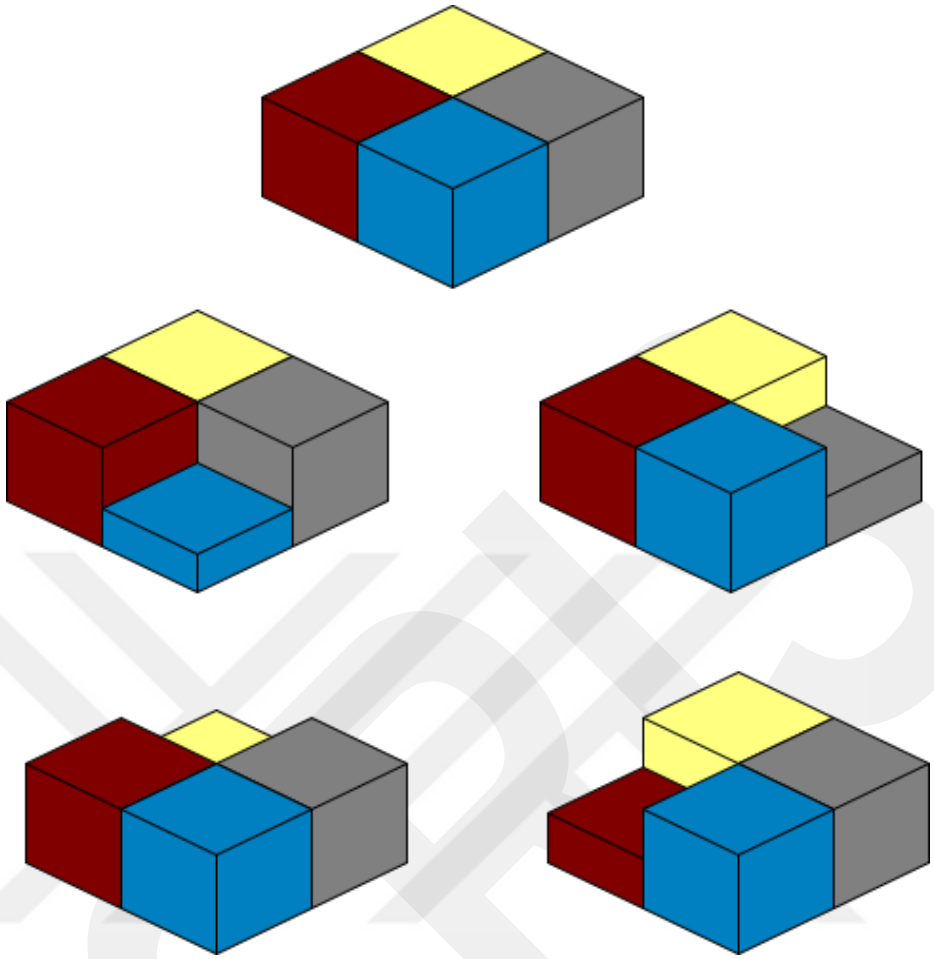


Figure 2.2 A schematic of a four-material processing approach, where each color signifies a distinct material. To enable advanced device fabrication, it is important to selectively etch one material without affecting the shapes or edges of the other three [18].

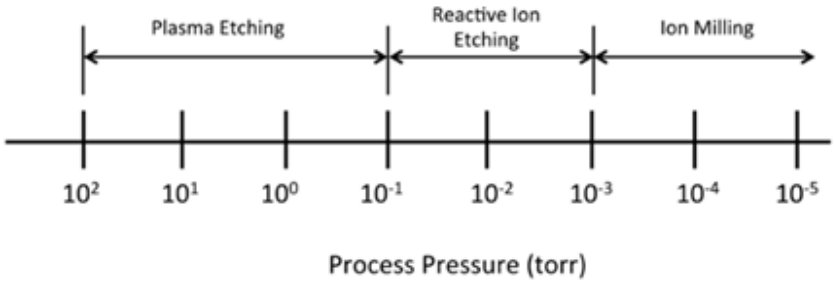


Figure 2.3 Variety of dry etching methods and their dependence on process pressure [21].

Reactive Ion Etching

RIE, or ion-assisted etching, integrates physical and chemical processes to achieve material removal [17]. Parallel plate reactors are commonly utilized for applications necessitating ion bombardment. In symmetrical low-pressure configurations, the plasma potential is elevated, resulting in both electrodes being subjected to energetic ion bombardment [22]. In this method, reactive species interact with the substrate material only when the surface is activated by the impact of incident ions from the plasma. These ions disrupt the surface by breaking chemical bonds, facilitating the reaction between the material and the reactive species [17]. RIE processes commonly employ gases containing halogens,which are Group VII elements, including fluorine, chlorine, bromine, and iodine, chosen for their strong electronegativity and high reactivity, which make them especially effective in driving etching reactions [21].

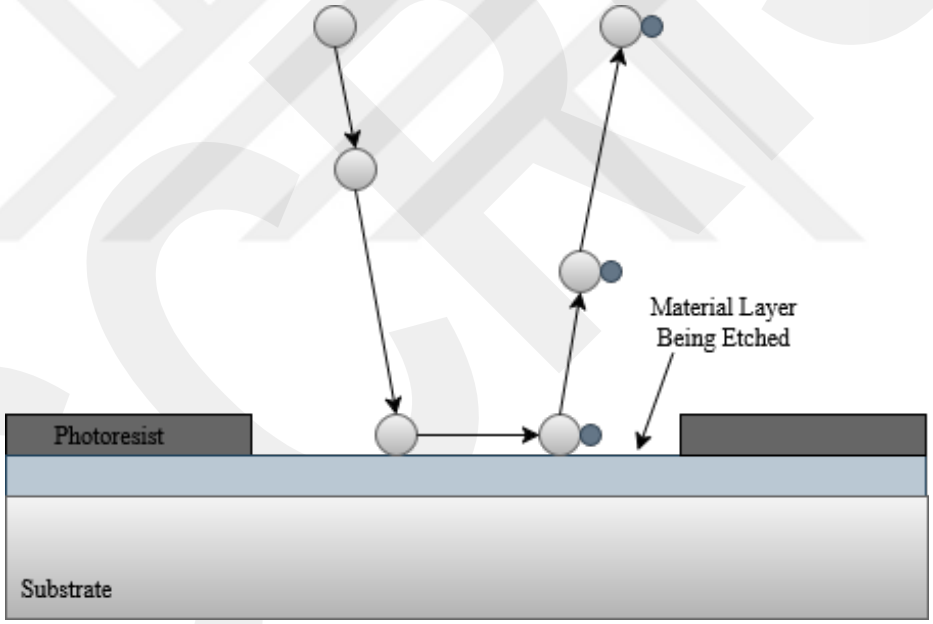


Figure 2.4 Illustration of the six steps involved in plasma etching. Step 1: process gases are broken into chemically reactive species in plasma; Step 2: diffusion of reactive species to substrate surface; Step 3: absorption of reactive species onto material layer; Step 4: reaction between reactive species and material layer; Step 5: desorption of reaction by-products; Step 6: diffusion of by-products [21].

Ion Milling

Ion milling is a purely physical etching technique that employs accelerated inert ions, such as Ar^+, which strike the substrate surface perpendicular to its plane to remove material. This process typically operates under low-pressure conditions (approximately 10^{-4} to 10^{-3} Torr) [17,21]. The primary characteristics of ion milling include its low etch rates (on the order of a few nanometers per minute) and poor selectivity, which is typically close to a 1:1 ratio for most materials. Consequently, this technique is generally suited for etching very thin layers [17]. In contrast, high-pressure plasma etching (10^{-1} to 5 Torr) relies on highly reactive species to chemically react with the target material. The resulting volatile by-products diffuse away, exposing new material to further etching. Directionality in plasma etching can be achieved through techniques such as sidewall passivation [17].

The ion milling process typically involves several steps:

1. Loading the wafer into the ion mill.
2. Configuring process parameters, including rotation speed, angles, and beam current/voltage settings.
3. Processing the wafer for a defined duration.
4. Repeating configuration and processing steps as required by the recipe.
5. Removing the wafer from the ion mill after processing.

Ion milling systems use an ion source to generate ions, which are accelerated through an electric field by a series of grids set at specific voltages. This creates a focused ion beam that strikes the wafer surface to dislodge material physically. The wafer is mounted on a rotating fixture that can tilt to different angles relative to the incoming ion beam, allowing precise control of the etching angle. A shutter mechanism can shield the wafer from the ion beam until milling is initiated [23].

The system also incorporates a Particle Beam Neutralizer (PBN) control mechanism to influence the shape and distribution of the ion beam as it travels toward the wafer

surface. The wafer is cooled using a flowcool system to prevent thermal damage during milling, which directs helium gas behind the wafer at a controlled flow rate. The helium gas is indirectly cooled by a water-cooling system. The helium cooling gas is separated from the vacuum chamber of an ion mill by a vacuum-sealed o-ring. Such integrated cooling maintains wafer thermal stability during etching [24].

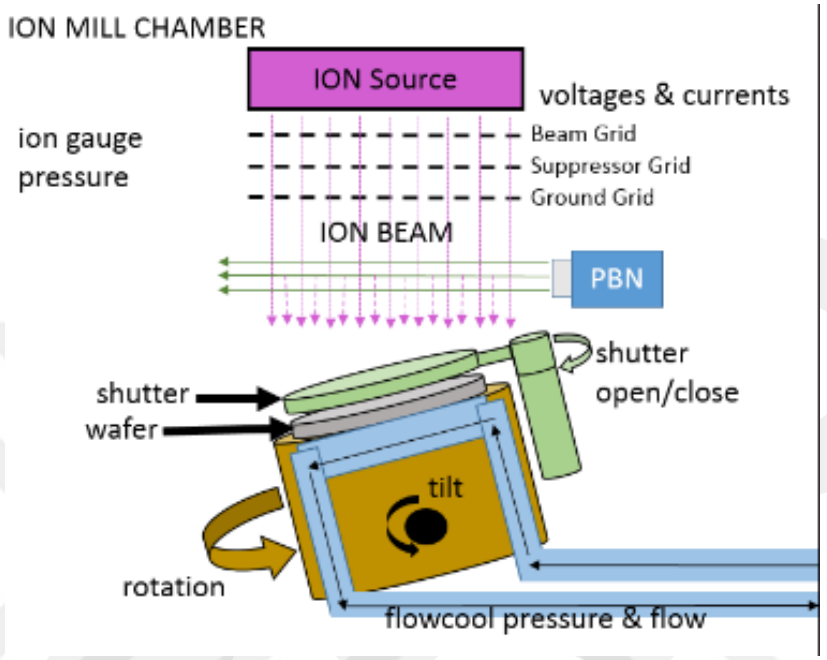


Figure 2.5 Overview of ion mil etching system [24].

Plasma Etching

The majority of dry etching methods rely on plasma-based processes [17]. Plasma-based techniques have been employed to produce fine-scale etched features in silicon integrated circuits for nearly five decades [19]. Plasma etching is a fundamental process in the semiconductor industry and is integral to producing electronic devices. For the precise transfer of a patterned mask into an underlying thin film, two key conditions must be satisfied: (i) the etching process must proceed in a strictly directional (vertical) manner, and (ii) the mask must remain largely unaltered, without incurring substantial lateral erosion or faceting [25].

Plasma etching is conducted at relatively high process pressures, ranging from 10^{-1} to 10^{2} Torr. Under these conditions, the plasma constituents have shorter mean free paths and undergo multiple collisions before reaching the substrate. These collisions

cause the etching species to strike the substrate at various angles, resulting in a more isotropic etching profile. As a result, plasma etching is primarily governed by chemical reactions between the reactive plasma species and the exposed material rather than physical effects. Similar to wet etching, plasma etching exhibits limited directionality but demonstrates significant material selectivity [21].

Wet Chemical Etching

The etching silicon (Si) surfaces with fluoride-based solutions is of both technological and scientific importance, as it underpins many processes in advanced semiconductor fabrication. Depending on the etching conditions, it is possible to produce either atomically flat, hydrogen-terminated surfaces or hydrogen-terminated porous silicon (por-Si) [26,27].

Etching with KOH Potassium Hydroxide (KOH), as an alkali hydroxide, is one of the most commonly used silicon etchants in anisotropic wet etching techniques and is the most preferred silicon etchant in micromachining of silicon wafers. Anisotropic etching selectively etches the material at different rates depending on the crystallographic orientation of the substrate. In contrast, isotropic etching methods such as hydrofluoric acid (HF) etch at equal rates in all directions. The KOH etching method is particularly preferred in silicon wafer production due to its consistent performance, uniform etching properties, and cost-effectiveness [28].

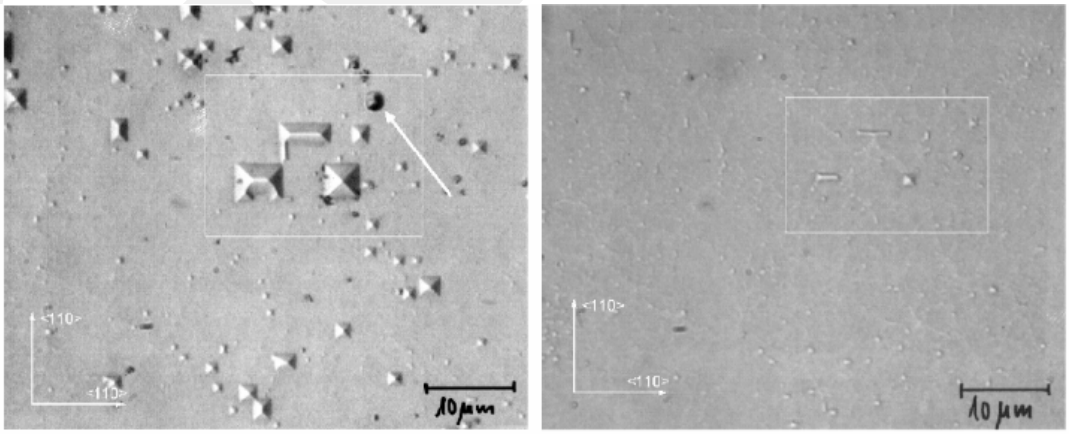


Figure 2.6 The micrographs of the same area of micropyramids in curved arrangements before and after re-etching with KOH [28].

2.3.3.3 Chemical Mechanical Polishing

Chemical Mechanical Polishing (CMP) combines mechanical and chemical removal techniques. CMP utilizes a polishing pad, abrasive slurry, and chemical additives that chemically react with the wafer surface to weaken bonds at the defective interface. The abrasive mechanical action simultaneously removes these weakened layers, producing highly smooth and defect-free surfaces. CMP's superior uniformity and surface finish are preferred for semiconductor device manufacturing, especially for advanced electronic device fabrication [29].

2.3.3.4 Laser-Based Methods

Recently developed laser-based methods include laser-induced periodic surface structuring (LIPSS) and photochemical etching for selective surface texturing and damage mitigation. Laser-based methods allow precise control and selective removal of surface damage with minimal collateral defect introduction. In particular, photochemical etching under controlled illumination of silicon wafers immersed in chemical solutions has demonstrated promising results for saw-damage removal with substrate integrity preservation for wafers used in high-efficiency photovoltaic devices [30].

Saw damage and its removal affect wafer quality and, thus, silicon-based device performance. Saw damage removal improves mechanical robustness and decreases surface defect density and electronic properties such as minority carrier lifetime and mobility. As such, advanced fabrication technologies involving photovoltaic and microelectronic devices rely heavily on optimized SDR techniques to achieve good performance, reliability, and reproducibility of silicon-based devices [31].

2.4 Silicon Wafer Characterization Methods

Silicon wafers constitute fundamental components of microelectronic and photovoltaic devices. Therefore, they are of prime structural, optical, chemical, and electrical importance for the performance and reliability of the final devices. Silicon wafer

characterization involves sophisticated analytical techniques to evaluate wafer quality, detect imperfections, and meet industry standards. Such characterization techniques may be structural, optical, chemical, or electrical methods, which all have different roles to play in assessing wafer attributes [32].

2.4.1 Structural Characterisation Methods

Structural characterization methods analyze the crystalline quality, surface morphology, and defects of silicon wafers.

- **X-Ray Diffraction (XRD):** Crystal orientation, lattice constants, and crystallinity of silicon wafers are analyzed using XRD. Based on Bragg's law, it reveals grain sizes and strain distributions through scattered X-ray intensity patterns [33].
- **Scanning Electron Microscopy (SEM):** SEM uses a focused electron beam to visualize surface morphology, grain boundaries, and defects like dislocations or contamination, supporting nanoscale quality control [34].
- **Transmission Electron Microscopy (TEM):** TEM enables imaging at the atomic scale, making it possible to observe internal features of the wafer such as dislocations, stacking faults, and grain boundaries in ultra-thin samples. This level of detail is essential for assessing the crystalline quality of the material [35].
- **Atomic Force Microscopy (AFM):** AFM scans wafer surfaces with a sharp probe to measure surface roughness and uniformity at sub-nanometer resolution, aiding in yield optimization [36].

2.4.2 Optical Characterization Methods

Optical characterization techniques examine optical properties, including reflectance, absorption, and bandgap characteristics, essential for photovoltaic and optoelectronic applications.

- **Reflectance and Transmittance Spectroscopy:** These optical techniques measure the reflected and transmitted light through silicon wafers. The results indicate anti-reflection coating performance, optical bandgap, and absorption properties, which are critical for photovoltaic and optoelectronic design [37].

- **Photoluminescence (PL) Spectroscopy:** PL analyzes photon emission from radiative recombination after optical excitation. Emission intensity and spectra reveal defect density, doping uniformity, and minority carrier lifetime—key indicators of wafer quality and solar cell efficiency [38].

- **Fourier Transform Infrared (FTIR) Spectroscopy:** FTIR identifies chemical bonds and impurities by measuring infrared absorption at specific characteristic frequencies. This measurement technique enables precise quantification of impurities such as oxygen, carbon, and hydrogen, which plays a critical role in assessing and ensuring the overall quality of the material [39].

2.4.3 Chemical Characterization Methods

Chemical characterization methods reveal wafer purity and impurity levels. Characterization results are essential to meet the fabrication requirements.

- **Secondary Ion Mass Spectrometry (SIMS):** SIMS uses a focused ion beam to eject and analyze secondary ions from the wafer surface, enabling precise detection of impurity and dopant profiles down to ppb levels. It is essential for doping accuracy and contamination monitoring [40, 41].

- **X-Ray Photoelectron Spectroscopy (XPS):** XPS is used to determine the elemental composition and chemical states of wafer surfaces by analyzing the kinetic energy of electrons emitted when the material is exposed to X-rays. It provides crucial data on surface chemistry, oxidation states, and interface properties [42].

2.4.4 Electrical Characterization Methods

Electrical characterization techniques quantify electrical properties, such as carrier lifetimes, resistivity, mobility, and doping uniformity.

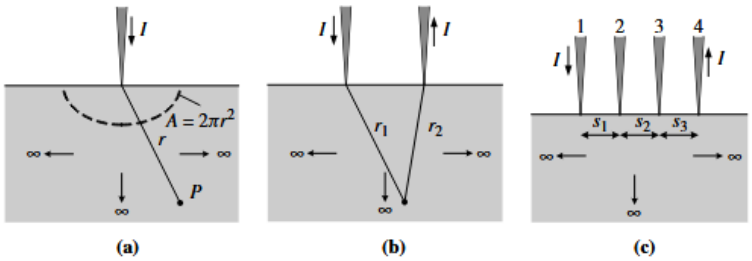


Figure 2.7 (a) one-point probe, (b) two-point, and (c) collinear four-point probe showing current flow and voltage measurement [43].

- **Four-Point Probe Method:** This technique measures sheet and wafer resistivity using four aligned probes, current flows through the outer probes while voltage is sensed between the inner ones. It enables accurate, non-destructive assessment of doping levels and electrical uniformity [43].

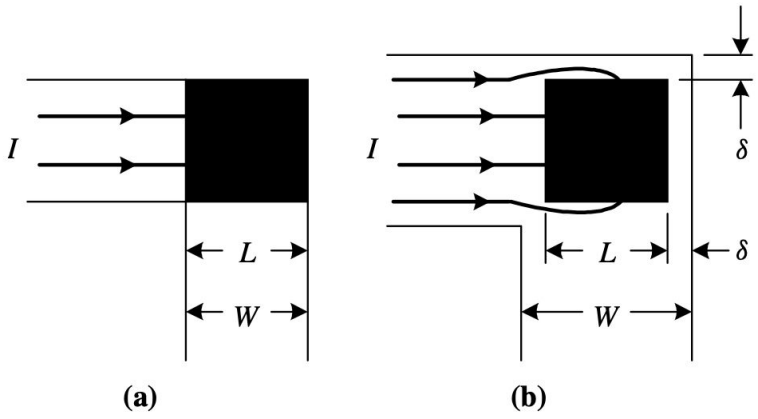


Figure 2.8 Four-terminal contact resistance test structures. (a) Ideal with only lateral current flow,
(b) showing current flowing into and around the contact. The black area is the contact area [43].

- **Hall Effect Measurement:** By applying a magnetic field perpendicular to current flow, Hall voltage reveals carrier concentration, mobility, and resistivity. These parameters are vital for evaluating doping efficiency and electrical performance in silicon wafers [43].

- **Minority Carrier Lifetime Measurement:** Techniques like microwave photoconductive decay (μ-PCD) and quasi-steady-state photoconductance (QSSPC) measure how long minority carriers survive before recombination. Longer lifetimes indicate better material quality, guiding wafer selection, passivation, and defect control in photovoltaic applications [44].

The characterization of silicon wafers involves structural, optical, chemical, and electrical analyses. Together, these techniques ensure that the wafers meet the requirements of high-performance microelectronic and photovoltaic devices. Accurate wafer characterization enables optimization of the fabrication process, facilitates the detection and reduction of defects, and ensures adherence to high-quality manufacturing standards. As a result, detailed wafer characterization is essential in semiconductor manufacturing, as it has a direct influence on the performance, reliability, and market readiness of silicon-based devices [45, 46].

2.5 Junctions, Solar Cells, and Photodetection Based on Silicon Wafers

Silicon wafers form the backbone of modern semiconductor technologies, particularly in solar energy conversion and optical detection systems. The properties of junctions created on silicon substrates fundamentally determine the operational efficiency of photovoltaic devices (solar cells) and photodetectors. This section describes the principles, fabrication methods, and performance implications of silicon-based junctions, solar cells, and photodetectors [45, 47].

2.5.1 Semiconductor Junctions in Silicon

A semiconductor junction is the region where two materials, either two semiconductors or a semiconductor and a metal, with distinct electronic properties come into contact. The presence of these junctions is fundamental to the operation of electronic and optoelectronic devices, as it significantly influences charge carrier dynamics, electrical conductivity, and the device's optical response [45, 47].

2.5.1.1 p-n Junctions

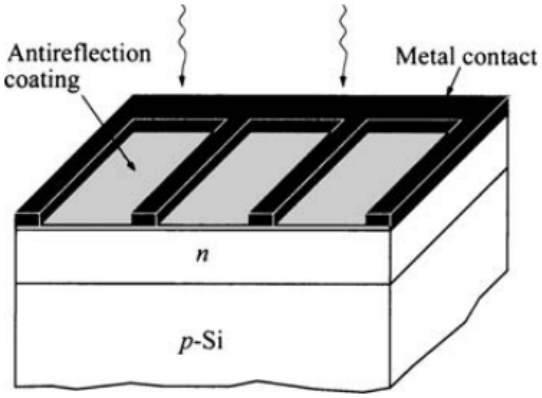


Figure 2.9 Schematic illustration of a silicon-based p–n junction solar cell [47].

The most widely employed junction in silicon technology is the p-n junction, consisting of a p-type semiconductor joined with an n-type semiconductor. Silicon wafers are typically doped with impurities such as boron (p-type) or phosphorus (n-type) to adjust their conductivity [47]. When these two differently doped silicon regions come into contact, electron-hole pairs diffuse across the interface. This diffusion establishes a depletion region where a built-in electric field forms, opposing further diffusion [45, 48].

Under equilibrium conditions, the built-in potential stabilizes, creating a rectifying junction. The rectification behavior is essential for diode applications, including photodiodes, LEDs, and photovoltaic cells. The electronic and optical performance of p-n junctions strongly depends on wafer characteristics, doping uniformity, and surface purity [47].

2.5.1.2 Schottky Junctions

Another widely studied junction is the Schottky junction, formed at the interface between a semiconductor (such as silicon) and a metal (e.g., graphene, gold, or aluminum). Unlike the p-n junction, the Schottky junction lacks a depletion region on both sides. Instead, depletion primarily occurs in the semiconductor adjacent to the metal-semiconductor interface [49].

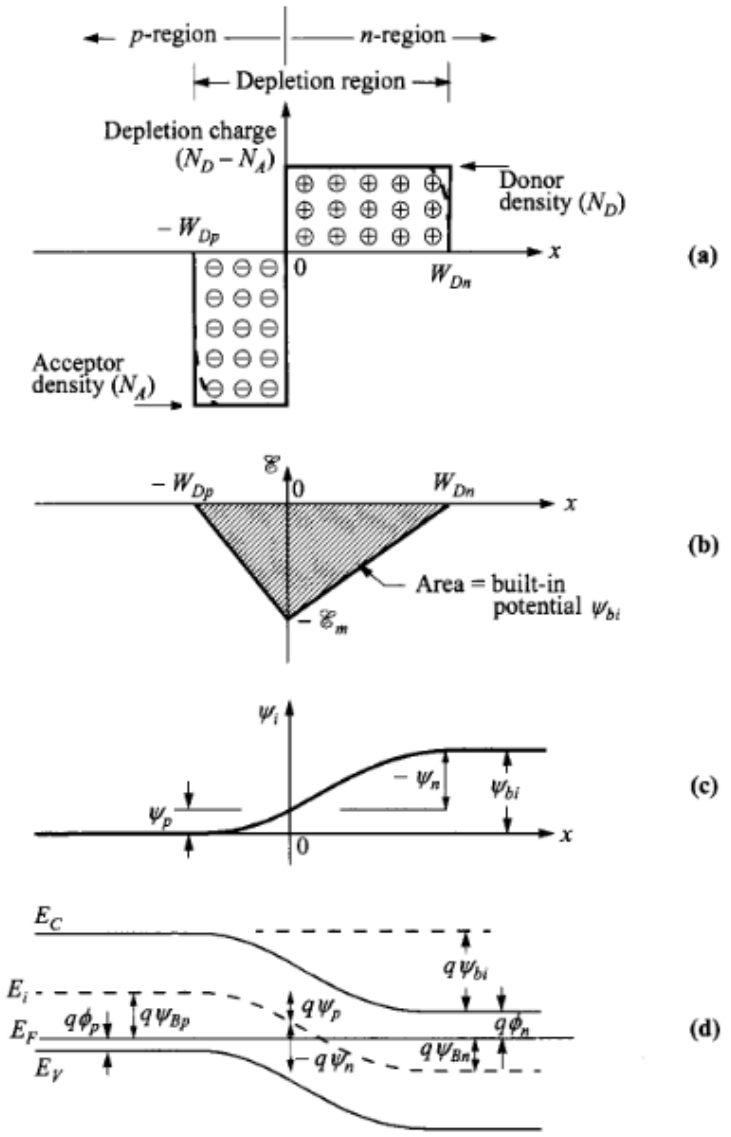


Figure 2.10 p–n junction in thermal equilibrium.
(a) Distribution of space charge across the junction; dashed lines illustrate deviations from the depletion approximation.
(b) Electric field profile within the depletion region.
(c) Variation of electrostatic potential, where ψ_{bi} represents the built-in potential.
(d) Energy band diagram corresponding to the junction [47].

The key parameters influencing Schottky junction properties are the metal work function and semiconductor electron affinity. The performance of Schottky devices depends critically on silicon wafer purity and surface quality, as defects or contaminants directly influence Schottky barrier height, affecting the diode's rectifying behavior and leakage currents [50].

2.5.1.3 Metal-Insulator-Semiconductor (MIS) Junctions

Metal-Insulator-Semiconductor junctions introduce a thin insulating layer (usually silicon dioxide, SiO_2) between the metal contact and the silicon wafer [47]. This insulator passivates the semiconductor surface and helps reduce recombination losses and leakage currents. MIS junctions exhibit superior control over interface properties and are widely used in high-performance photovoltaic and photodetection applications [46].

2.5.2 Silicon-Based Solar Cells

Silicon-based solar cells convert incident solar radiation directly to electrical energy using the photovoltaic effect [51]. They are typically based around p-n, Schottky, or MIS junctions on silicon wafers [52].

2.5.2.1 Working Principle of Silicon Solar Cells

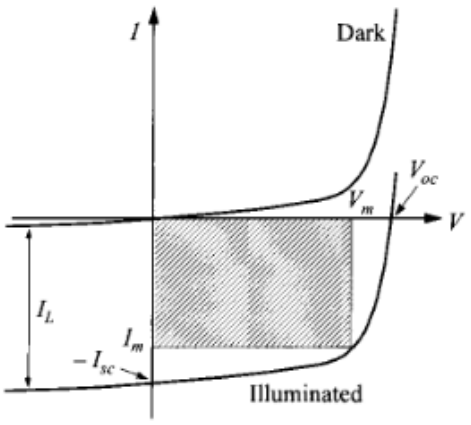


Figure 2.11 Current–voltage (I–V) characteristics of a solar cell under illumination. The point corresponding to the maximum power output is shown [47].

Solar cells function by absorbing photons from incident sunlight, generating electron-hole pairs within the silicon wafer [53]. When photons with energy higher than silicon's bandgap ($\approx 1.1\,eV$) reach the wafer, electrons are excited from the

valence band to the conduction band, leaving behind holes [45]. The built-in electric field at the junction separates these generated carriers: electrons are driven toward the n-type region, while holes migrate toward the p-type region, resulting in the generation of a photocurrent [54].

2.5.2.2 Performance Parameters and Silicon Wafer Quality

The key performance parameters for solar cells include open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}), fill factor (FF), and conversion efficiency (η) [45, 47]. These parameters significantly depend on silicon wafer properties:

- **Open-Circuit Voltage (V_{oc}):** Directly proportional to the built-in voltage and junction quality. Wafer purity, doping concentration, and surface passivation quality critically influence V_{oc} [45].
- **Short-Circuit Current Density (J_{sc}):** It depends on wafer absorption characteristics and minority carrier lifetime. High-quality silicon wafers, with fewer defects and higher purity, exhibit superior J_{sc} due to reduced recombination losses [47].
- **Fill Factor (FF):** The junction quality, wafer resistivity, and contact resistance determine the fill factor. Low series resistance and high shunt resistance, combined with quality wafer processing, ensure high FF [45].
- **Efficiency (η):** It reflects overall solar cell quality, which is heavily dependent on wafer characteristics, junction quality, and surface passivation effectiveness [45, 47].

2.5.2.3 Solar Cell Structures

- **Monocrystalline Solar Cells:** Constructed from high-purity monocrystalline silicon wafers with a uniform crystal structure, good electronic properties, and high efficiency [47].

- **Polycrystalline Solar Cells:** Produced from multicrystalline silicon wafers, economically beneficial, although typically less efficient due to grain boundaries that introduce recombination sites [66].
- **Silicon Schottky Solar Cells:** Recently reported graphene-silicon Schottky junctions with good conductivity and transparency have shown promising performance owing to simplified fabrication processes and lower production costs [45, 47].

2.5.3 Photodetection Process in Silicon Wafers

Photodetection is the process where optical signals (photons) are converted to electrical signals that can be measured [55]. Good bandgap and excellent electronic properties make silicon wafers popular in photodetection systems [56]. For detector efficiency and performance optimization, a detailed photodetection process description of a silicon detector is important [57].

The photodetection process of silicon wafers has three stages:

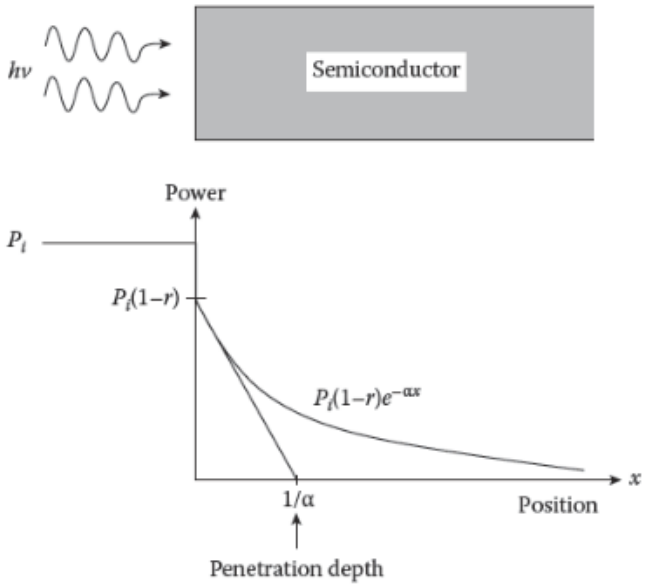


Figure 2.12 Optical absorption of in a semiconductor [55].

- **Photon Absorption:** When photons of sufficient energy (greater than the silicon bandgap energy of approximately 1.1 eV) strike the silicon wafer surface, their

energy is absorbed [58]. This absorption depends on wafer thickness, surface texturing, reflection coatings, and incident photon wavelength [59]. Silicon absorbs photons in the visible and near-infrared spectral ranges and is suitable for many photodetection applications [60].

- **Carrier Generation:** Absorbed photons attract electrons from the silicon valence band to the conduction band, leaving holes [61]. Such electron-hole pairs act as photogenerated carriers. The optical properties and quality of the silicon wafer depend on incident light intensity and wavelength and the number of photogenerated carriers. Wafer quality permits efficient carrier generation without recombination losses [62, 63].
- **Carrier Collection and Detection:** A semiconductor junction (p-n or Schottky) creates an internal electric field within the silicon wafer [64]. This internal field drives electrons and holes toward opposite electrodes when generating new electron-hole pairs. Those separated charges give off a measured electrical current or voltage proportional to the incident optical intensity, completing the photodetection process [65].

A few critical factors determine the photodetection process efficiency in silicon wafers:

- **Carrier Lifetime:** The lifetime of photogenerated carriers in a wafer affects detector sensitivity. Better-quality silicon wafers with fewer defects show longer carrier lifetimes, improving detection efficiency [47].
- **Junction Quality:** A well-engineered junction improves carrier collection efficiency by providing an optimal built-in electric field: doping profiles, wafer cleanliness, and passivation quality influence junction quality [66].
- **Surface Passivation:** Wafer surfaces and interfaces are subjected to surface passivation techniques to remove recombination sites, extending carrier lifetimes and improving photodetection efficiency [43, 66].
- **Wafer Thickness & Absorption Properties:** Wafer thickness and optical properties should be optimized to maximize photon absorption and carrier generation with minimum recombination [43, 47].

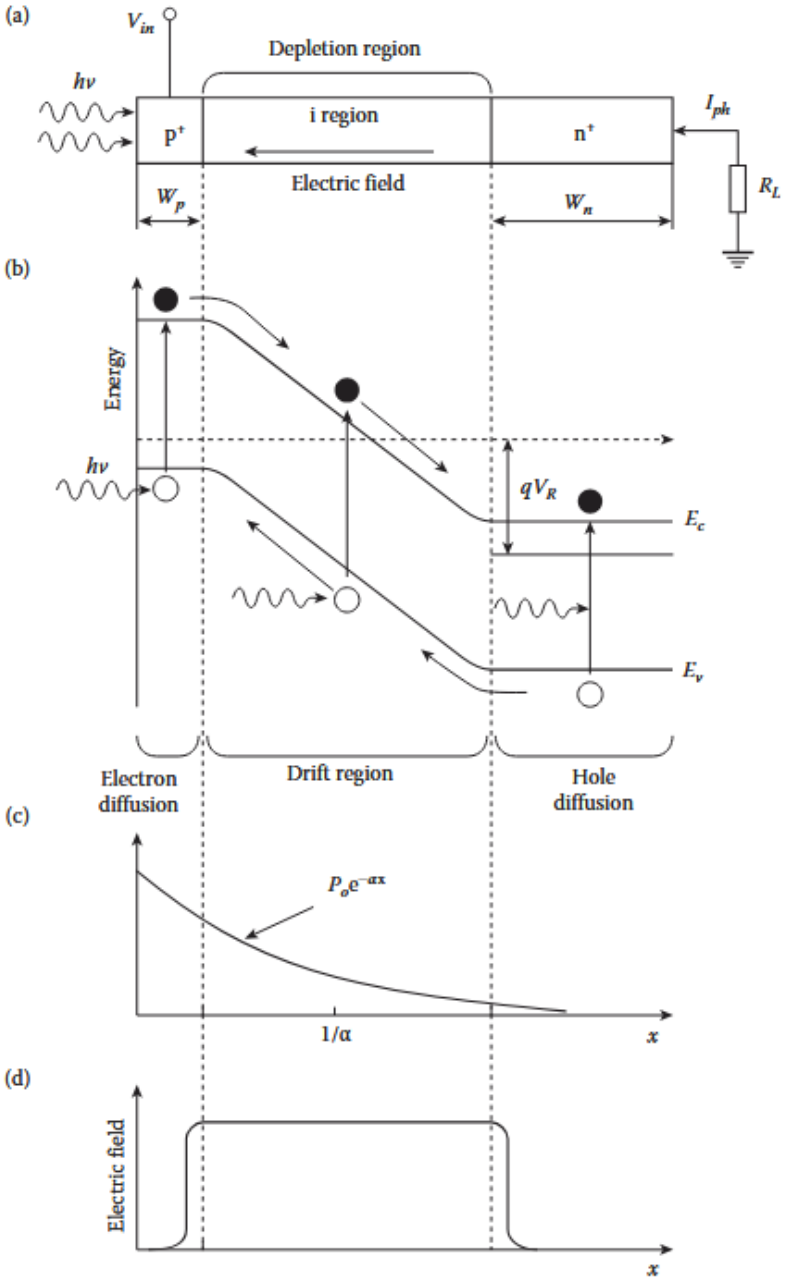


Figure 2.13 p–i–n photodiode:
(a) Layered device structure,
(b) Corresponding energy band configuration,
(c) Photogenerated carrier distribution,
(d) Electric field variation across the device [55].

Silicon-based photodetection process performance is evaluated by parameters such as:

- **Quantum Efficiency (QE):** Defined as the ratio of generated electron-hole pairs to incident photons directly influenced by wafer purity and surface passivation [66].
- **Responsivity (R):** Refers to how effectively a device converts incoming light into electrical current. It mainly depends on how long the charge carriers can survive before recombining and how efficiently the junction separates and collects them [43].
- **Dark Current and Noise:** Dark current is the small electrical current that flows through a device even when no light is present. It can be caused by imperfections in the wafer, unwanted impurities, or leakage at the junction. Lower dark current levels usually indicate a higher-quality wafer and lead to better signal clarity and lower noise in the device [47].
- **Response Time:** The response time of the detector to optical signals changes related to carrier mobility and wafer quality [66].

2.5.4 Influence of Silicon Wafer Quality on Device Performance

Silicon wafer purity, doping uniformity, crystal quality, and surface characteristics affect the performance of photovoltaic and photodetection devices. For high-efficiency photovoltaic conversion and sensitive photodetection, longer minority carrier lifetimes and diffusion lengths are required [55]. Also, lower dark currents are critical for improving photodetection sensitivity and noise performance [67]. Optimized junction formation increases built-in potentials, carrier separation efficiency, and device performance [68].

Junction creation, solar cell functionality & photodetection principles are closely related to silicon wafer characteristics. To obtain the best performance and reliability from silicon-based solar cells and photodetectors, both the design of the junctions and the quality of the silicon wafers need to be carefully optimized. This close relationship between wafer quality and device design remains a major area of research, as it plays a key role in advancing solar energy technologies and improving optical sensing systems [45, 47].

2.6 Light Trapping for Silicon-Based Solar Cells

One of the principal challenges silicon-based photovoltaic technologies face is maximizing light absorption within the active semiconductor layer [69]. Silicon possesses an indirect bandgap with a relatively low absorption coefficient, particularly for photons near the band-edge energy [70]. The efficiency of different light-trapping methods has been researched and optimized. Light trapping leads to increased photon absorption and photogenerated current, resulting in increased efficiency for silicon-based solar cells [71].

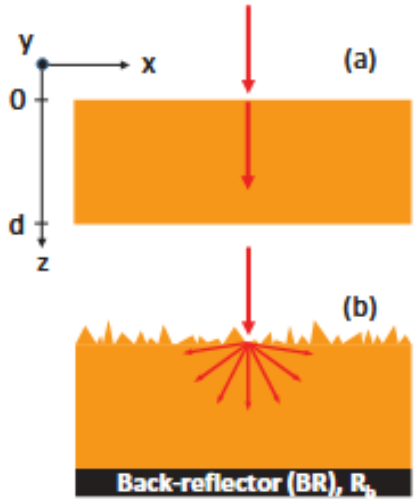


Figure 2.14 Illustration of the structural configuration of (a) a solar cell with a single layer enabling single-pass photon absorption, and (b) a configuration incorporating a Lambertian scatterer at the front surface and a rear-side reflector, resulting in Lambertian light trapping [71].

Crystalline silicon c-Si remains the most common material for photovoltaic technologies due to its abundance, stability, and mature manufacturing processes [72]. However, due to its indirect bandgap nature, silicon shows relatively poor optical absorption. High-efficiency silicon solar cells usually need thick wafers (100-300 μm), increasing material consumption and cost [68, 73].
Effective light trapping strategies allow thinner silicon layers to be used while maintaining or enhancing the absorption of incident photons. Therefore, optimized light-trapping schemes directly enhance the economic viability and the efficiency of silicon-based photovoltaics [74].

Light trapping confines incident photons within the semiconductor material, thus increasing the optical path length and the absorption probability in silicon solar cells. Effective light trapping involves manipulating photon propagation through several internal reflections, diffraction, and scattering within the silicon wafer [75]. Fundamental considerations for light trapping are:

- Increasing Optical Path Length: The path length with the probability of photon absorption within the semiconductor layer is increased by photon confinement [75].
- Reducing Reflection Losses: Surface reflections at interfaces are minimized to reduce photon entry into silicon wafers [46 ,75].
- Enhanced Scattering and Diffraction: Surface and internal textures scatter photons, enhancing interactions within the semiconductor and absorption [75].

There are four techniques developed and studied for improving light trapping in silicon-based solar cells.

Surface texturing creates micro-or nanostructures on silicon wafer surfaces for internal reflection, scattering, and photon confinement [76]:

Alkaline Texturing (Random Pyramids): Monocrystalline silicon wafers are anisotropically etched using alkaline solutions (potassium hydroxide, KOH) to form pyramidal structures with dimensions typically 3–10 μm. Randomly oriented pyramids significantly reduce reflectance and increase the internal optical path length by causing multiple internal reflections, thereby substantially enhancing photon absorption [74].

Isotropic Texturing: Multi-crystalline silicon wafers, which have varied crystallographic orientations, require isotropic texturing methods involving acidic solutions (HF/HNO_3). This method creates a random, irregular surface texture that effectively scatters incoming photons [75, 76].

Nano-texturing and Black Silicon: Advanced surface textures at the nanoscale, such as black silicon fabricated via metal-assisted chemical etching (MACE), RIE, or laser-induced texturing, demonstrate extremely low reflectance (<5%) across a broad wavelength range. Such nanostructures significantly increase light absorption through efficient scattering and trapping at the nanoscale [79].

Anti-reflection coatings minimize front-surface reflectance. Single-layer or multi-layer thin films (commonly silicon nitride, SiN_x, or titanium dioxide, TiO_2) are designed with carefully tuned refractive indices and thicknesses to induce destructive interference of reflected photons, maximizing photon coupling into the silicon wafer. In combination with textured surfaces, ARCs achieve reflectance values below 5% [80].

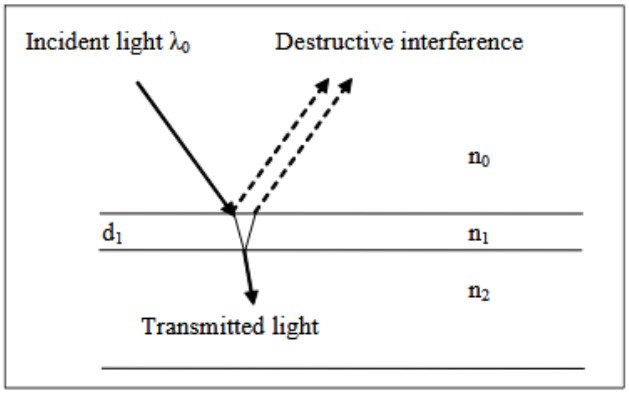


Figure 2.15 Diagram illustrating the working principle of a single-layer anti-reflection coating (ARC) [75].

The back surface of silicon wafers is often covered with reflective layers (metal or dielectric) to trap light [81]. Introducing a back reflector significantly increases internal reflections within the wafer, particularly for photons with lower absorption probabilities (near-bandgap photons). The rear surface passivation and reflection improve carrier collection by reducing recombination, consequently enhancing cell efficiency [68].

Plasmonic structures integrate metallic nanoparticles (silver or gold) to enhance the local electric field intensity through surface plasmon resonances [82]. These plasmonic effects increase light coupling into silicon and improve absorption, particularly in thin-film silicon cells [83]. Currently, mostly experimental, plasmonic approaches point to great promise for further silicon solar cell performance improvement [84].

2.6.1 Advanced Light Trapping Approaches

2.6.1.1 Photonic Crystal Structures

Periodic dielectric structures, designed at scales comparable to the wavelength of light, help control how photons move and are confined within the silicon. These structures enhance optical absorption by introducing diffraction and wave-guiding effects, which effectively increase the light's path length inside the material and improve overall absorption efficiency [85].

2.6.1.2 Laser-Based Texturing (LIPSS, PCE)

LIPSS and PCE are recently reported techniques for silicon wafer texturing. They allow precise control of nanostructure dimensions and periodicity for better light trapping and absorption efficiency. Photosynthetically etched inverted nanoholes have shown good trapping performance and improved solar cell efficiency [86].

2.6.2 Evaluation Criteria for Light Trapping

Several key metrics are commonly used to assess the effectiveness of different light-trapping schemes:

- **Surface Reflectance:** Lower reflectance values indicate efficient photon entry into the silicon wafer, increasing internal absorption [45].
- **Internal Quantum Efficiency (IQE):** IQE measures the efficiency of photogenerated charge carriers that reach electrodes, which is closely related to how effectively absorbed photons contribute to photocurrent generation [46].
- **Optical Path Length Enhancement Factor:** A quantitative measure of how often the photon path length is increased by trapping structures compared to a flat reference wafer [45].
- **Short-Circuit Current Density (Jsc) Enhancement:** An increase in measured J_{sc} demonstrates that improved light trapping translates directly into higher cell performance [85].

2.6.3 Influence of Silicon Wafer Properties on Light Trapping

Applied light-trapping methods are affected by wafer characteristics:

- **Wafer Thickness and Doping:** Optimal thickness and doping concentrations allow good photon absorption and carrier collection efficiency [43].
- **Surface Quality and Passivation:** Qualitative surface passivation permits low carrier recombination at textured surfaces, resulting in better absorption and electrical performance [43, 68].
- **Material Purity and Crystal Quality:** Reducing crystal defects and improving material purity help extend the lifetime of minority carriers, which is essential for maximizing the effectiveness of light trapping in silicon-based devices [68].

2.7 Surface Texturing Methods for Silicon-Based Solar Cells

Enhanced photovoltaic device performance via surface texturing of silicon wafers is a widely used strategy. This reduces reflection losses and increases optical path length within the active silicon layer, enabling higher photon absorption. Various approaches

with different capabilities and limitations have been developed for effective surface texturing, including chemical texturing, MACE, direct laser texturing, and PCE [88, 89].

2.7.1 Chemical Texturing

Chemical texturing is a basic and widely used process for improving the surface roughness of silicon wafers, which in turn improves the optical absorption capacity of photovoltaic devices [68].

- **Monocrystalline Silicon (Anisotropic Etching):** Texturing is typically performed using alkaline solutions, such as potassium hydroxide [68]. This method is known as anisotropic etching because the etch rate varies depending on crystallographic orientation. (100)-oriented silicon wafers etch more rapidly than (111)-oriented planes, leading to the formation of pyramid-like structures bounded by the slower-etching (111) facets. These randomly distributed pyramids reduce surface reflectance from over 30% to less than 10% [45].
- **Multi-crystalline Silicon (Isotropic Etching):** Due to the varying orientation of grains in multi-crystalline wafers, anisotropic texturing is not feasible. Instead, isotropic etching methods are used with acidic solutions such as HF-HNO_3 mixtures. In this process, silicon is first oxidized by nitric acid and then etched by hydrofluoric acid [45, 74]. The resulting irregular surface scatters incident light, which enhances light absorption and reduces reflection. However, isotropic etching generally results in higher reflectance compared to anisotropic pyramid texturing [74].

2.7.2 Metal-Assisted Chemical Etching

MACE is a wet etching technique that creates nanoscale textures on silicon using noble metal nanoparticles, such as silver or gold, as catalysts in HF and H_2O_2 solutions [90]. The process starts with the deposition of metal particles on the silicon surface, which catalyze local oxidation when immersed in the etching solution. The resulting

oxide is then removed by HF, forming nanostructures like nanowires or nanopores depending on process parameters [90, 91]. MACE is valued for its simplicity, low cost, and precise control over structure dimensions; however, residual metal particles can degrade electrical performance, requiring post-cleaning steps [92].

2.7.3 Direct Laser Texturing

Laser texturing is very flexible and precise. These direct laser pulse techniques use controlled textures on silicon surfaces.

- **Laser-Induced Periodic Surface Structuring:** LIPSS uses ultra-short laser pulses (femtosecond or picosecond) to create periodic nanostructures on silicon through controlled ablation. The pattern formation depends on parameters like pulse duration, wavelength, polarization, fluence, and scanning speed. It effectively lowers surface reflectivity and works for both mono- and multi-crystalline wafers [93, 94]. While offering good control and orientation independence [93], it may cause subsurface damage, requiring thermal annealing or passivation afterward [94].
- **Photochemical Etching:** PCE is a surface texturing method that combines laser irradiation with wet chemical etching. Photon-generated electron-hole pairs trigger the etching process without external electrical bias [95]. This makes it possible to selectively remove material within a chemical solution using only laser energy, without the need for additional masks or electrical bias [96].

2.8 Surface Structuring of Silicon via Photochemical Etching

2.8.1 Introduction to Photochemical Etching for Silicon

Photochemical Etching is a novel and controllable surface structuring technique for silicon substrates that applies to photovoltaics, sensors, and microelectronics applications. Like chemical or electrochemical methods, photochemical etching is driven locally by photon-induced charge carrier generation. This approach provides excellent spatial control over surface modifications and fabricates nano- and

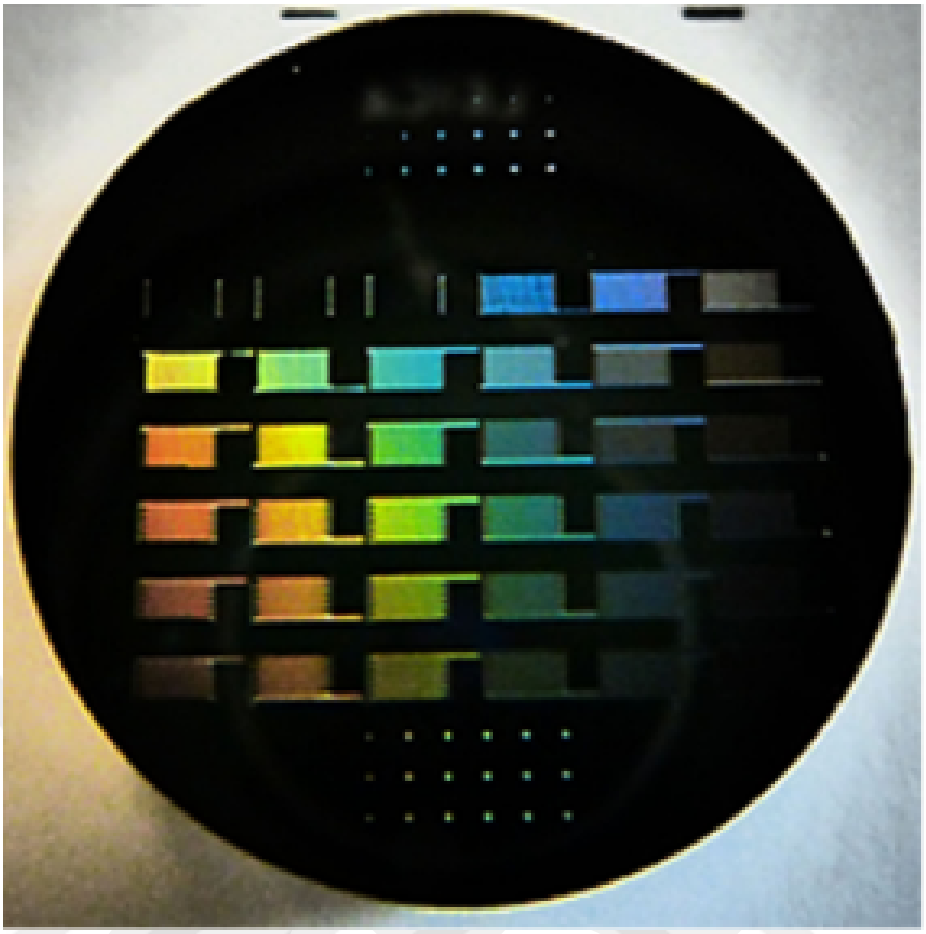


Figure 2.16 The colors on the steel sample arise from optical diffraction of ambient light at laser-generated LSFL [93].

micro-structured surfaces without external electrical bias.

The technique involves immersing a silicon wafer in a fluoride-based etchant solution, typically a mixture of hydrofluoric acid and an oxidizing agent such as hydrogen peroxide, while simultaneously illuminating the surface with a continuous-wave (CW) laser. Upon absorption of photons, electron-hole pairs are generated within the silicon substrate. The photogenerated holes (h^+) migrate to the silicon surface, where they initiate oxidation reactions that are subsequently followed by chemical etching of the oxidized silicon species by HF. This process permits highly localized, selective material removal, particularly suited for producing light-trapping nanostructures on silicon surfaces [97].

Given the indirect bandgap nature of silicon and its relatively weak absorption of longer-wavelength light, the selection of photon energy, typically through the use of 532 nm lasers, is critical to ensure efficient carrier generation close to the surface. Photochemical etching is thus a maskless, bias-free alternative to more conventional lithography-based surface patterning techniques [98].

2.8.2 Mechanism of Silicon Surface Etching in PCE

In the photochemical etching process, photogenerated carriers are produced and used. When a photon with energy greater than the bandgap of silicon is absorbed, an electron is excited to the conduction band, leaving a hole in the valence band. The separation and migration of these carriers are crucial: holes must reach the surface before recombination occurs [98].

At the silicon-electrolyte interface, the holes participate in oxidation reactions. The oxidation of silicon leads to the formation of Si-OH bonds, which are subsequently attacked and dissolved by fluoride ions from HF to form soluble hexafluorosilicate ions (SiF_6^{2-}) [26]. The chemical reactions governing this process can be summarized as follows:

$$Si + 6HF + h^+ \rightarrow H_2SiF_6 + H_2 \uparrow + H_2O \tag{2.1}$$

In this reaction, hydrofluoric acid not only provides fluoride ions necessary for dissolving the oxidized silicon but also maintains the surface in a reactive state by continuously removing reaction by-products. The role of hydrogen peroxide is primarily as an oxidizer, assisting in the supply of additional holes via chemical reactions, thus sustaining the etching process even when photon flux alone may be insufficient.

Since the etching proceeds only where sufficient photogenerated holes are available, the process inherently provides spatial selectivity. Illuminated areas experience significantly faster etching compared to shaded regions, enabling the fabrication of patterned surfaces when combined with appropriate optical masking techniques, such as those provided by digital micromirror devices (DMDs).

2.8.3 Optical Setup for Photochemical Etching

The optical setup is an important parameter in the PCE process, influencing the etching precision and quality. An advanced optical setup would typically include:

- **Laser Source and Optics:** A 532 nm diode-pumped solid-state (DPSS) continuous-wave laser is commonly used due to strong absorption by silicon. Laser power is typically kept between 200–700 mW to control etching depth and structure. Optical components like mirrors, lenses, and beam expanders shape and guide the beam for uniform illumination [99].

- **Digital Micromirror Device (DMD):** The DMD gives flexible, real-time control over how the laser beam hits the wafer. Each tiny mirror, about 16 micrometers wide, can tilt to either reflect the beam onto the surface or away from it. This makes it easy to adjust the pattern and area being etched on the fly, allowing for very accurate and customizable processing [99, 100].

- **Chemical Setup and Wafer Positioning:** The wafer is placed in a polypropylene container filled with HF, H_2O_2, and H_2O solution. A stable wafer holder ensures proper alignment and uniform exposure during the etching process [99].

2.8.4 Parameters Controlling PCE

PCE depends on a combination of factors that work together, such as the preparation of the chemical solution, the laser's power and exposure time, and the surrounding environmental conditions. These variables collectively influence etch rate, surface morphology, and nanostructure uniformity.

Etching Solution Composition: The solution typically consists of HF, H_2O_2, and deionized water. HF dissolves the oxidized silicon layer, while H_2O_2 chemically generates holes, initiating oxidation. A higher HF concentration increases the etch rate but may cause surface roughness and feature non-uniformity. Similarly, excess H_2O_2 can lead to over-oxidation, while insufficient amounts slow the process. DI water adjusts overall reactivity, more water slows reactions and improves control, while less water increases speed but risks non-uniformity [101, 102].

Laser Parameters: The laser's wavelength, power, and exposure time determine carrier generation and energy delivery. A 532 nm laser is ideal due to its strong absorption in silicon. Increased power raises the hole generation rate, accelerating etching, but excessive power can cause thermal effects like melting or ablation [103]. Longer exposure deepens structures but may reduce resolution due to carrier diffusion and local chemical depletion [104]. Since CW lasers provide constant illumination, exposure time becomes the key factor for etch control.

Temperature and pH: Reaction kinetics are sensitive to temperature and acidity. Moderate heating enhances etching speed, but uncontrolled temperatures can compromise uniformity and surface quality. Maintaining a low pH ensures active fluoride ions and continuous dissolution of oxidized silicon, making pH stability essential for consistent etching performance [105].

Process Optimization: Balancing all parameters, chemical concentrations, laser intensity, exposure time, and environmental conditions, enables precise fabrication of structures such as nanoholes or inverted pyramids. When optimized, the process yields highly uniform and reproducible features, improving optical absorption and device performance.

2.9 Photochemical Etching-Based Solar Cell Fabrication and Efficiency Enhancements

Constant need for better performing and lower cost photovoltaic technologies drove considerable development in surface structuring of silicon wafers [106]. Since silicon, despite its favorable abundance and electronic properties, possesses an indirect bandgap resulting in limited optical absorption, especially near the band edge [107], enhancing light trapping is crucial to achieving high-performance devices. One of the most promising approaches to address this limitation is surface texturing [108, 109, 110].

Among the developed texturing methods, photochemical etching is unique in combining precision, scalability, and compatibility with known semiconductor pro- cessing technologies [111]. In the PCE process, surface texturing is achieved by laser-driven chemical reaction, and there is no need for complex lithography or high-energy pulsed laser systems [111, 112]. It allows for the fabrication of engineered nanostructures, enhancing optical absorption while maintaining good electrical properties [112, 113, 114].

This section presents a detailed overview of the solar cell fabrication process based on PCE, discusses the influence of surface morphology on device efficiency, explains subsequent device patterning and electrode fabrication steps, and compares PCE with other advanced texturing techniques such as black silicon formation.

2.9.1 Morphology of Etched Surfaces: Inverted and Upright Features

Surface morphology plays a critical role in determining both the optical and electrical performance of silicon solar cells. The morphology of surfaces textured via PCE can vary depending on laser power, chemical composition, and exposure duration [115, 116]. Under optimized conditions favoring uniform hole generation and moderate etching rates, the process produces inverted features such as nanoholes, inverted pyramids, or concave pits [117, 118].

Periodic inverted nanopyramid (INP) structures have been shown to substantially improve light trapping and enhance the optical performance of monocrystalline silicon solar cells. These textures are typically fabricated using UV nanoimprint lithography, in which a silicon master mold is first patterned via laser interference lithography and subsequently transferred through reactive ion etching and anisotropic KOH wet etching. The resulting inverted geometry minimizes surface reflectance and increases the probability of multiple internal reflections, thereby extending the optical path length within the active layer and contributing to higher power conversion efficiency [122].

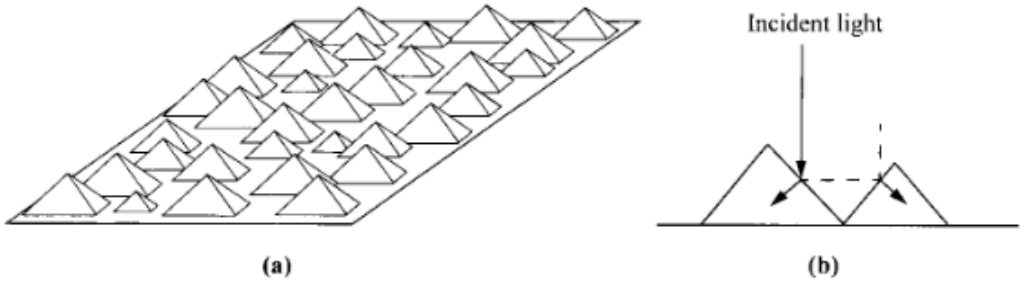


Figure 2.17 (a) Cell with a textured surface featuring pyramid-like structures.
(b) Illustration of the optical path demonstrating light trapping to minimize reflection [47].

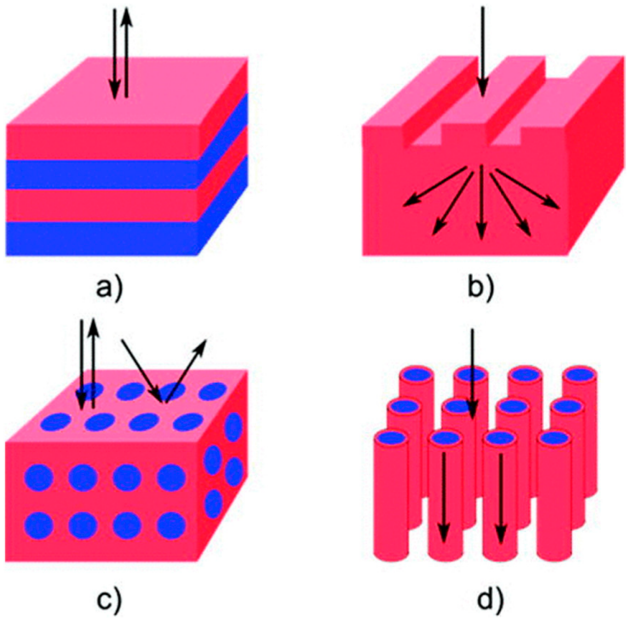


Figure 2.18 Schematic representations of nanophotonic structures for improving solar cell efficiency, including (a) 1D Bragg stacks, (b) 2D gratings, (c) photonic crystals, and (d) nanowires [122].

Inverted structures are highly favorable for photovoltaic applications because they produce an effective graded refractive index profile between air and silicon, significantly reducing surface reflectance and increasing photon absorption. Light entering the inverted features experiences multiple internal reflections, enhancing the optical path length and improving the probability of absorption even for long-wavelength photons [119, 120, 121].

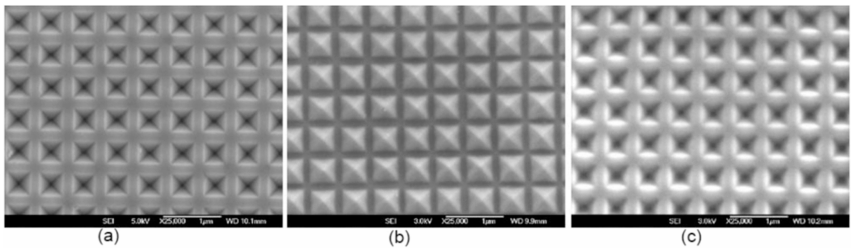


Figure 2.19 SEM images of (a) inverted nanopyramids on the Si master mold, (b) upright replicas after first imprint, and (c) inverted structures on the solar cell after second imprint [122].

In contrast to inverted nanostructures, upright geometries such as nanopillars or spikes tend to exhibit higher surface recombination due to their sharp edges and increased surface area. This leads to a trade-off where optical gains are offset by electrical losses. Such inverted morphologies are, therefore, generally used in high-efficiency solar cells as they offer a good compromise between the optical and electric properties [122, 123].

2.9.2 Electrode Deposition

Once the active regions of the device are defined, metallic contacts are deposited to facilitate charge collection. A grid pattern of fine metal fingers is applied on the front surface to minimize optical shading while maintaining low series resistance. Standard methods include screen- printing silver pastes followed by sintering or vacuum deposition techniques such as evaporation or sputtering combined with photolithographic lift-off [47, 125]. Ensuring good electrical contact is critical for PCE-treated surfaces because the nanostructured surface can introduce contact resistance if metal deposition is not optimized [68].

The rear surface typically receives a full-area metal contact, often aluminum or silver. In more advanced solar cell designs, a rear passivation layer, often made of silicon

dioxide (SiO_2) or silicon nitride (Si_3N_4), is added between the silicon and the metal contact. This layer helps reduce charge carrier recombination, leading to structures such as passivated emitter rear locally diffused (PERL) cells or passivated rear contact solar cells [126].

Establishing high-quality electrical contacts is crucial not only for reducing resistive losses but also for preserving long minority carrier lifetimes. This becomes even more effective when combined with the smoother, well-textured surfaces created through PCE, which help minimize surface recombination [127].

2.9.3 Efficiency Enhancements from Photochemical Etching

Photochemical etching contributes to solar cell efficiency improvements through multiple interconnected mechanisms:

2.9.3.1 Reduced Surface Reflectance

The dense inverted nanostructures created via PCE drastically reduce surface reflectance, typically lowering it from ~30% for flat silicon to below 10% across a broad spectral range. Enhanced light trapping increases the generation of electron-hole pairs, leading to a higher short-circuit current density (J_{sc}) [74, 128].

2.9.3.2 Enhanced Light Trapping

Beyond mere anti-reflection, the geometry of inverted nanoholes promotes multi-pass photon trajectories within the silicon absorber. This effect is significant for wavelengths near the silicon absorption edge (900–1100 nm), where absorption is intrinsically weak [5, 129].

2.9.3.3 Improved Carrier Collection

The relatively smooth, inverted profiles produced by PCE minimize the surface area compared to spiky structures, reducing surface recombination velocities. This effect

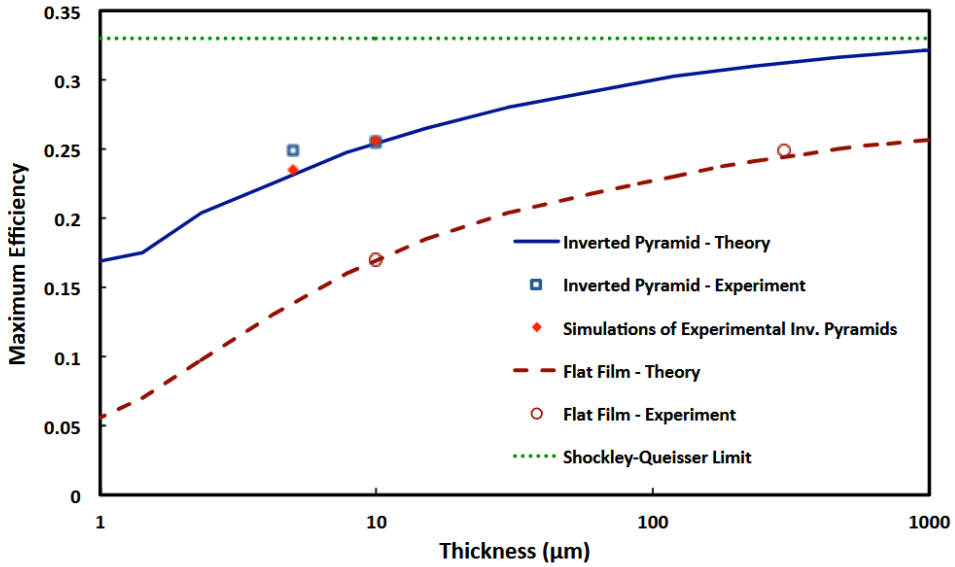


Figure 2.20 Maximum efficiency under normal incidence as a function of absorber thickness is shown for simulated inverted nanopyramid structures (blue solid line) and flat silicon films (brown dashed line), each incorporating anti-reflection coatings of 90 nm and 63 nm SiN_x, respectively [5].

preserves minority carrier lifetimes, leading to higher open-circuit voltages (V_{oc}) and improved fill factors (FF) [68, 130].

2.9.3.4 Compatibility with Simple Fabrication

PCE structures do not need complex gas-phase reactors or ultrafast lasers like black silicon. This simplicity leads to lower manufacturing costs and easy integration into existing solar cell production lines [128, 131].

Because of these combined advantages, PCE-treated solar cells routinely exhibit several percentage points higher efficiency than planar or simply textured counterparts, particularly when integrated with modern passivation and contact technologies [128, 132].

2.9.4 Comparison Between PCE and Black Silicon Solar Cells

2.9.4.1 Fabrication Process

Black silicon is often fabricated by femtosecond laser irradiation in reactive atmospheres or by metal-assisted chemical etching. These techniques produce extremely high-aspect-ratio structures, typically resembling dense forests of nano-spikes [119, 133].

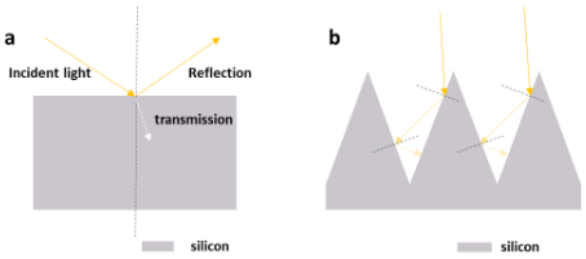


Figure 2.21 The reflection performance of (a) polished silicon and (b) black silicon [134].

In contrast, PCE employs relatively simple liquid-phase chemistry combined with continuous-wave laser illumination to generate low-aspect-ratio, inverted features without needing reactive gases, noble metals, or ultrafast lasers [134, 128].

2.9.4.2 Surface Morphology and Optical Properties

Black silicon achieves extraordinarily low surface reflectance, sometimes below 1%. However, its spiky structures present significantly larger surface areas, leading to higher recombination rates unless very high-quality passivation layers are applied. Without excellent passivation, black silicon cells can suffer from lower V_{oc} and degraded overall efficiencies [88, 135, 137].

While slightly higher in reflectance (~8–10%), PCE surfaces offer a superior balance between light trapping and electrical quality. The moderate increase in surface area results in lower recombination, maintaining high carrier lifetimes without demanding extremely advanced passivation [128, 136].

2.9.4.3 Scalability and Cost

Black silicon fabrication involves expensive equipment and additional passivation steps. In contrast, PCE is naturally low-cost and compatible with industrial scale-up using simple wet chemistry and inexpensive CW lasers . All these attributes make PCE an economically viable option for the mass production of high-efficiency silicon solar cells [98, 119, 131].

Photochemical etching represents a highly promising surface modification technique capable of driving the next generation of silicon photovoltaic technologies. By enabling the fabrication of precisely engineered inverted nanostructures, PCE enhances light trapping, reduces reflection losses, and maintains favorable electrical properties, all essential for maximizing solar cell efficiency [128].

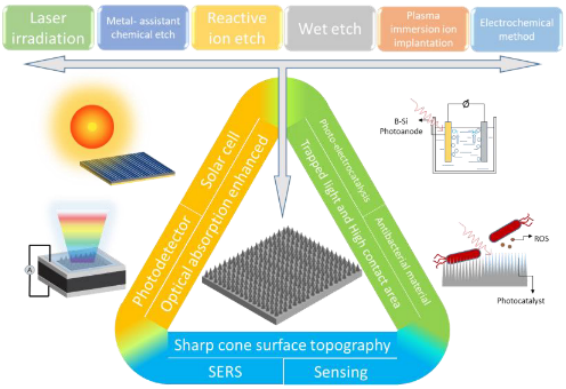


Figure 2.22 The overview of fabrication methods, characteristics and corresponding applications [134].

When integrated with advanced photolithography and optimized metallization processes, PCE-treated surfaces contribute to developing high-performance, scalable, and cost-effective solar cells. Compared to black silicon technologies, PCE offers a more balanced, manufacturable approach, avoiding many complexities and drawbacks associated with extremely high-surface-area structures [131].

As photovoltaic technologies improve, photochemical etching is poised to become an important link between laboratory-scale efficiency and commercial-scale mass production.

2.10 Efficiency Improvements from Surface Texturing in Silicon Solar Cells

Surface texturing is an established method for improving the efficiency of silicon-based solar cells [76]. Due to silicon's relatively high refractive index (~3.5 at 600 nm) and indirect bandgap, a planar, polished silicon surface reflects a significant portion of incident sunlight, up to 30% across the visible spectrum, resulting in substantial optical losses [136, 137, 138]. Texturing techniques aimed at suppressing reflection and enhancing light trapping have evolved over decades from simple chemical etching to advanced laser-based and photochemical methods [76, 131].

This section reviews reported efficiency values and experimental outcomes for flat and textured silicon surfaces, comparing various texturing methods, and emphasizes why PCE offers superior outcomes in contemporary silicon photovoltaic research.

2.10.1 Efficiency Measurements for Flat Silicon Solar Cells

While essential for establishing baseline performance, flat, untextured silicon wafers suffer significant optical losses due to Fresnel reflection at the air-silicon interface. In early generations of silicon solar cells fabricated on polished substrates, short-circuit current densities (J_{sc}) were typically limited to values around 20–25 mA/cm^2, resulting in efficiencies of 10–14% under AM1.5G standard conditions [45, 139]).

Reflectance measurements on polished silicon surfaces commonly show average reflectance values of 30–35% across the 300–1100 nm wavelength range [68]. Due to these high reflection losses and weak light trapping, photon absorption in flat wafers is inadequate, particularly for long-wavelength photons near the silicon bandgap edge.

Flat surfaces don't help much when it comes to scattering light or extending its path inside the wafer. As a result, photons either get absorbed in a single pass or simply escape, which greatly limits how efficiently the device can convert light, especially in thinner silicon layers [47].

Therefore, despite the high material quality of polished silicon, flat surfaces alone fall short in achieving competitive energy conversion efficiency [94].

2.10.2 Efficiency Improvements Through Surface Texturing

By adding textured patterns to the surface of silicon wafers, incoming light is scattered more effectively, helping it travel longer paths within the material and bounce around more, this boosts the chances of capturing and converting that light into energy. Various texturing strategies have been developed over the years, each offering distinct advantages and trade-offs between optical gains and electrical losses [117].

One widely used method is chemical anisotropic texturing. This approach employs alkaline solutions, typically KOH, to etch monocrystalline silicon wafers. The process exploits the anisotropic etching rates of different crystallographic planes to form micron-scale pyramidal structures [45]. The resulting surface morphology reduces reflectance to around 10–12% without the need for anti-reflection coatings [47]. Solar cells fabricated with chemically textured monocrystalline wafers achieve short-circuit current densities of approximately 35–37 mA/cm^2 and conversion efficiencies typically around 18–20% [68]. However, for multi-crystalline silicon, this technique is less effective, as random grain orientations inhibit the uniform formation of pyramids.

Another notable technique is MACE, which utilizes noble metal catalysts to locally enhance silicon etching in HF-based solutions [134]. This method produces nanowire arrays or nano-conical structures, achieving reflectance values below 5%. Solar cells incorporating MACE textures can reach J_{sc} values above 38 mA/cm^2 and efficiencies around 19–20%, provided that effective surface passivation is applied [79, 90]. However, concerns regarding residual metal contamination and the complexity of cleaning processes present challenges to long-term device stability and process reproducibility.

A more advanced approach is femtosecond laser texturing, often used to produce black silicon. This method involves using femtosecond laser pulses in reactive gas atmospheres (e.g., SF_6), resulting in nano-spiked surfaces with extremely low reflectance, typically around 1–2% [140]. While black silicon offers excellent optical performance, its high surface area significantly increases surface recombination. This limits the open-circuit voltage (V_{oc}) unless advanced passivation layers, such as atomic layer deposited Al_2O_3, are implemented [74, 101]. When optimized, black silicon

solar cells have demonstrated efficiencies of 21–22% in laboratory settings [141]. However, bringing this method to large-scale production is still a challenge because of its complexity and high manufacturing costs.

2.10.3 Comparative Discussion

Efficiency outcomes between flat and textured surfaces show the benefit of surface texturing. High reflectance and low light-trapping flat silicon surfaces limit photovoltaic performance. Chemical texturing and MACE significantly improve but introduce material compatibility and contamination problems.

Black silicon demonstrates the optical ideal of near-perfect absorption but suffers electrical penalties due to increased surface recombination, requiring additional processing complexity.

In contrast, PCE strikes an effective balance:

- Achieves significant reflectance reduction,
- Maintains low surface recombination due to inverted nanostructure geometry,
- Utilizes scalable and straightforward processing technologies,
- Eliminates the need for noble metals or high-vacuum equipment.

This combination explains why PCE-treated silicon surfaces consistently provide the best efficiency results in recent photovoltaic research. PCE is also intrinsically compatible with continuous-wave laser systems and standard wet processing tools for industrial applications.

CHAPTER 3
METHODOLOGY AND EXPERIMENTAL SETUP

In this study, a single-step photochemical etching technique was employed to fabricate inverted nanohole structures on crystalline silicon wafers. The process relies on the simultaneous application of CW laser irradiation and a chemically reactive etchant solution composed of HF, H_2O_2, and deionized (DI) water.

3.11 Process Principles and Etchant Design

The implementation of a single-step photochemical etching method for the fabricating inverted nanohole structures on crystalline silicon surfaces stems from the need for a streamlined, lithography-free, and environmentally benign approach that enables fine control over surface topography at the nanoscale. Conventional techniques such as photolithography, RIE, or laser ablation often require cleanroom facilities, expensive equipment, vacuum systems, and multi-stage processing steps, collectively increasing fabrication costs and limiting scalability. In contrast, the PCE technique leverages the localized energy deposition of a continuous-wave laser beam in combination with a liquid-phase chemical etchant, facilitating spatially selective material removal under ambient pressure and temperature conditions. This makes the method not only economically attractive but also compatible with large-area processing and high-throughput manufacturing, especially in photovoltaic and optoelectronic device applications where uniformity and reproducibility are of paramount importance.

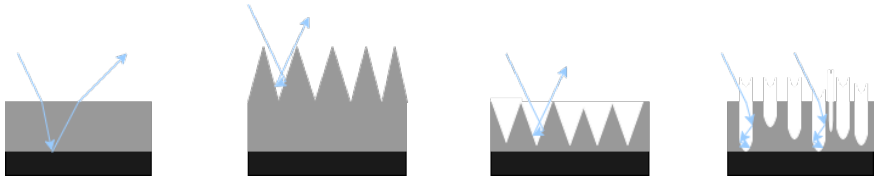


Figure 3.23 Schematic comparison of different surface texturing techniques on silicon wafers. From left to right: (a) flat wafer; (b) upright pyramids; (c) inverted pyramids; (4) inverted nanoholes.

The composition of the chemical etching solution was carefully engineered to exploit the synergistic behavior of HF, H_2O_2, and DI water under laser-assisted excitation. HF serves as the primary etchant, selectively removing silicon dioxide by forming soluble hexafluorosilicate (SiF_6^{2-}) complexes, thus enabling continuous dissolution of the laser-oxidized silicon surface. H_2O_2 functions as a mild oxidizing agent that photochemically generates valence band holes and facilitates the oxidation of crystalline silicon, particularly in non-irradiated regions. This promotes etch uniformity and lateral propagation of nanos- tructures across the wafer surface. Unlike nitric acid (HNO_3), which is commonly employed in metal-assisted or chemical polishing techniques, H_2O_2 decomposes cleanly into water and oxygen, thereby reducing the generation of hazardous nitrogen oxides and minimizing contamination risks that could compromise the optical or electronic properties of the etched surface. The inclusion of DI water plays a multifaceted role in this system. It acts as a diluent to modulate the etch rate and control the reaction kinetics while reducing the vapor pressure of HF, which is a critical factor in maintaining a stable chemical environment over prolonged etching durations. Additionally, DI water suppresses rapid solvent evaporation, which could otherwise lead to unwanted concentration gradients, non-uniform etching, and degradation of the optical path due to condensation or vapor accumulation on the laser-transmitting window. The overall formulation of the etchant thus supports a self-limiting, optically driven reaction front, enabling precise control over nanohole geometry and surface coverage without the need for complex masking, alignment, or post-processing. In summary, the selected chemical system forms the basis of a robust and scalable nanostructuring platform in conjunction with controlled laser irradiation. Its simplicity, environment-friendliness, and process flexibility make it an attractive approach to fabricating anti-reflective surfaces, advanced light-trapping structures, and next-generation photovoltaic interfaces. The following section provides schematics

and parametric analyses of etching dynamics and morphological outcomes of this technique.

3.11.1 Solution Optimization and Compositional Effects

To better understand how the chemical composition affects etching performance, surface texture, and overall uniformity, a set of carefully planned experiments was carried out by adjusting the amounts of HF, H_2O_2, and deionized water were varied. Each solution was prepared with different proportions of these three components, and the corresponding etching behavior was closely monitored. The goal was to identify the minimum effective concentrations of each chemical required to initiate and sustain the photochemical reaction responsible for forming inverted nanohole structures on crystalline silicon surfaces.

It was observed that no significant etching occurred in solutions where the HF content was below 25%, the H_2O_2 ratio was less than 20%, or the DI water fraction exceeded 55%. These results suggest that both the oxidation and etching reactions must occur simultaneously and at sufficient intensities to generate a stable and continuous dissolution front. In particular, HF removes oxidized silicon by forming soluble SiF_6^{2-} complexes. At the same time, H_2O_2 provides the necessary oxidation potential by generating valence band holes, thereby initiating silicon surface oxidation even outside the laser-irradiated zones.

As the HF concentration was increased to 35% and the DI water content was lowered to 45%, the onset of etching became more evident. The surface features produced under these conditions were observed to be deeper and more uniform, indicating that the lower HF dilution permitted a more aggressive chemical attack on the oxidized silicon layer. A more significant enhancement of etching performance was obtained by simultaneously increasing the HF / H_2O_2 ratio to 45% / 35%, respectively. These conditions led to more consistent nanohole formation across the wafer and a higher degree of structural regularity, as verified by scanning electron microscopy analysis.

The most reproducible and well-defined nanostructures were obtained using a solution of 50% HF, 35% H_2O_2, and 15% DI water. This composition resulted in deep, uniformly distributed inverted nanoholes with minimal surface roughness and high pattern fidelity. Consequently, this optimized mixture was selected for all subsequent etching experiments in the study. Table 3.1 summarizes the various solution compositions tested and the observed etching outcomes ranging from no reaction to complete and homogeneous nanostructuring.

Table 3.1 Optimization of Chemical Solution Compositions for PCE

Solution No.	**HF (%)**	**H_2O_2 (%)**	**DI Water (%)**	**Result**
1	25	20	55	Etching did not occur
2	35	20	45	Etching partially occurred
3	45	20	35	Etching occurred
4	45	35	20	Etching occurred
5	50	35	15	Etching occurred (most consistent)

While this formulation yielded the most favorable results for the specific process parameters used in this work, it should be noted that alternative ratios may be better suited for different target morphologies, etch depths, or application-specific requirements. As such, the chemical composition can be further tailored in future studies depending on the desired surface properties or device integration constraints.

(a) Etching did not occur (b) Etching partially occurred (c) Etching occurred (d) Etching occurred (Most convenient)

Figure 3.24 Comparison of surface morphologies at different etching stages.

3.12 Experimental Setup and Etching Mechanism

The experimental setup designed for single-step inverted nanohole photochemical etching was developed to provide precise spatial control over the interaction between optical excitation and the chemically reactive environment. The goal was to fabricate nanostructures on crystalline silicon surfaces using a lithography-free and ambient-pressure technique, relying solely on the photochemical compatibility between laser illumination and a tailored etchant solution. The complete system consists of a continuous-wave laser source, beam-shaping optics, a chemically inert reaction chamber, and temperature-controlled staging for process stability.

The etching mechanism is fundamentally governed by two concurrent processes: photo-induced surface oxidation and chemical dissolution. The 532 nm CW laser is used to locally excite the silicon substrate immersed in a solution of HF, H_2O_2, and deionized water. The incident photons generate electron-hole pairs within the silicon, where valence band holes (h^+) drive the oxidation of the silicon surface. Simultaneously, H_2O_2 assists in maintaining a uniform oxidation rate over the exposed and surrounding regions, while HF selectively removes the resulting silicon oxide by forming soluble SiF_6^{2-} complexes. This dynamic interaction between localized optical energy deposition and wet chemical reactivity allows for self-limiting, anisotropic nanohole formation without physical patterning or masking.

To ensure uniform etching over the target area, the wafer is placed flat in a shallow polypropylene (PP5) container filled with the etchant solution. A laser-transparent glass window is sealed on top of the container to allow safe and uniform laser delivery without allowing vapor escape or environmental contamination. This glass also acts as a protective barrier against HF fumes, which are highly reactive and can condense on optical surfaces if not appropriately managed. Therefore, careful sealing and isolation of the chemical chamber is critical for both safety and process reproducibility. All etching processes were carried out at room temperature (25 °C) without active stirring. The chemical solution remained static during laser exposure.

Laser power, exposure time, and beam diameter are the primary parameters influencing etch depth, nanohole diameter, and spacing. The reaction rate is highest in the illuminated zone due to the elevated generation of carriers, resulting in more pronounced etching directly under the laser focus. By contrast, regions further from the beam receive less photonic excitation and exhibit reduced or negligible etching, producing a controlled, high-contrast nanostructure pattern. The stability of the etchant solution over time is also a critical factor, as H_2O_2 can degrade and HF can volatilize, potentially altering the etch rate if not properly managed. For this reason, the solution is freshly prepared before each experiment, and the duration of exposure is limited to less than one hour.

The entire etching process is performed under ambient laboratory conditions without requiring inert atmospheres or vacuum systems, making the technique scalable and accessible. However, due to the volatile and hazardous nature of HF, all experiments are conducted within a certified fume hood, and appropriate personal protective equipment is worn at all times.

After covering the chemical and physical principles behind the etching system, the next section takes a closer look at the optical setup, explaining how the laser beam is aligned, expanded, and guided using mirrors and lenses to precisely target the silicon wafer.

3.12.1 Optical Setup

The optical system used in the SS-INH-PCE process was designed to deliver a spatially uniform, vertically incident laser beam onto the surface of a silicon wafer immersed in a reactive chemical solution. A 532 nm continuous-wave laser source serves as the primary excitation mechanism, chosen for its stable output and strong absorption characteristics in crystalline silicon. An experimental view of the optical setup and laser alignment near the chemical chamber is shown in Figure 3.26. The configuration, shown schematically in Figure 3.25, employs seven dielectric mirrors, a beam expander, a collimator, and a focusing system to precisely shape and guide the beam along a well-controlled optical path.

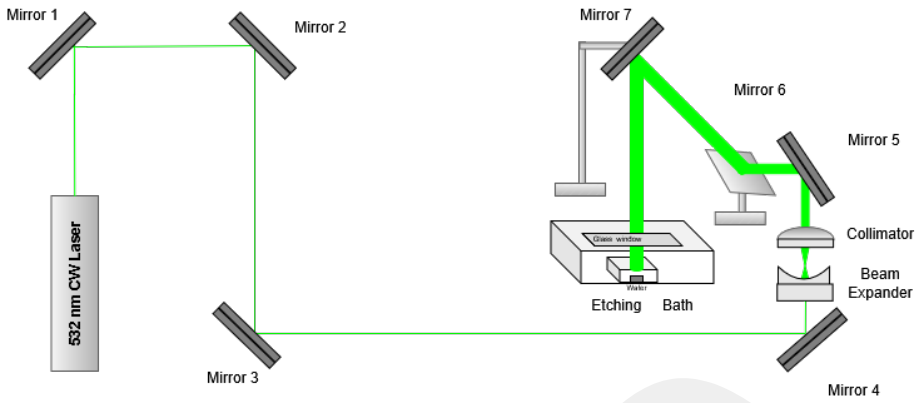


Figure 3.25 Schematic of the optical system including seven mirrors, a beam expander, collimator, and final focusing optics used to deliver the laser beam onto the wafer.

The laser beam first exits the CW laser module and encounters a series of four planar dielectric mirrors positioned in a horizontal plane. These mirrors are mounted on kinematic mirror mounts and strategically arranged to fold the beam path in a compact layout, preserving beam height and alignment while minimizing table space. After reflecting off the fourth mirror, the laser beam is directed into a beam expander followed by a collimator. The beam expander increases the diameter of the laser to reduce local power density and improve illumination uniformity. At the same time, the collimator realigns the diverging rays to ensure a near-parallel beam profile, which is critical for minimizing spot size distortion at the wafer surface.

Following collimation, the beam is reflected by a fifth mirror that redirects it toward a sixth mirror mounted at an oblique angle. This intermediate mirror guides the horizontally propagating beam toward the vertical direction. The sixth mirror then redirects the beam upward along the z-axis. This vertical segment is finally intercepted by a seventh and final mirror positioned above the reaction chamber, which reflects the beam downward at 90 degrees, directing it orthogonally toward the wafer surface.

The laser passes through a plano-convex focusing lens before entering the chemical container. The lens is positioned such that the laser beam is focused to approximately 1.6 cm in diameter when it reaches the wafer. This dimension was experimentally optimized to ensure uniform energy distribution across the exposed area. The chemical etchant's container is fabricated from HF-resistant polypropylene, and a square section on its upper surface has been manually removed and replaced with a glass window. This

laser-grade glass is chemically bonded to the container to allow optical transmission while preventing HF vapor escape.

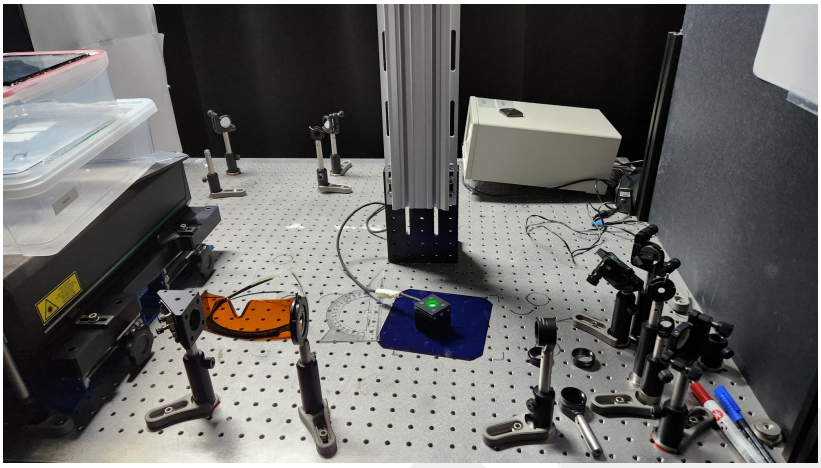


Figure 3.26 Experimental view of laser alignment and power measurement setup near the chemical chamber.

The wafer rests at the bottom of the container, submerged in a freshly prepared solution of HF, H_2O_2, and DI water. The vertically incident laser beam generates electron-hole pairs within the silicon substrate, initiating localized oxidation reactions. H_2O_2 sustains oxidation in both illuminated and surrounding regions, while HF rapidly dissolves the oxidized material, resulting in the formation of uniform inverted nanoholes.

Throughout the setup, optical components are aligned on a vibration-isolated optical table. Using dielectric-coated mirrors with high reflectivity at 532 nm minimizes reflective losses. Despite these optimizations, total power loss across the system was measured at approximately 35%, primarily due to surface reflections and slight scattering at the glass interface. Routine realignment procedures and cleaning protocols are implemented to maintain consistent beam quality between experiments.

To maintain homogeneous chemical activity in the etching bath, a magnetic stirrer is employed throughout the process. In the absence of stirring, the reaction tends to become self-limiting due to the localized accumulation of reaction by-products near the wafer surface. Continuous agitation ensures the uniform distribution of reagents and effective removal of etch products, thereby sustaining optimal reaction kinetics during laser exposure.

The entire system is operated under a certified fume hood to ensure laboratory safety, and the laser pathway is enclosed wherever feasible. Appropriate laser goggles rated for 532 nm are worn, and beam stops are installed beyond the final optical axis to prevent accidental reflections.

3.12.2 Power Measurement and Beam Profiling

Quantitative laser power and beam profile analysis are critical to understanding the energy interaction dynamics in the SS-INH-PCE process. The system is based on a frequency-doubled Nd:YAG laser source emitting both 1064 nm and 532 nm wavelengths. Only the 532 nm output is aligned and used for etching. In contrast, the unaligned residual 1064 nm component, visible in Figure 3.27, is negligible in power and has no practical effect on the delivered energy at the wafer surface.

Figure 3.27 Visual observation of residual 1064 nm infrared beam (unfocused) alongside the aligned 532 nm green beam.

The laser's output was set to 1 W at 532 nm. A calibrated optical power meter (Newport 1936-C) was used to measure the actual optical output directly at the laser head. As shown in Figure 3.28(a), a maximum output of 947.5 mW was recorded, revealing a 5% intrinsic loss likely due to internal beam splitting and second harmonic generation inefficiencies within the laser module.

Following this, the beam travels through a sequence of **seven** planar dielectric mirrors, a **beam expander** and a **collimator** before reaching the wafer. Each optical interface

(a) Measured laser power at the source (Newport 1936-C): 947.5 mW.

(b) Measured laser power at the wafer surface: approximately 500 mW.

Figure 3.28 Power measurements at two critical locations using a calibrated optical power meter. (a) shows the laser output directly at the source, while (b) shows the delivered power at the wafer surface after all optical and chamber-related losses.

introduces an estimated 3–4% power loss due to reflection and scattering. The beam is finally directed through two laser-grade glass windows mounted on the chemical etching chamber. Despite their high transmission at 532 nm, these windows contribute additional attenuation. Using the same power meter, a final power measurement was conducted directly above the wafer plane. As shown in Figure 3.28(b), the measured value was approximately 499.8 mW, indicating a total transmission loss of roughly 50% from the original laser output.

The breakdown of losses is as follows: approximately 35% cumulative optical loss due to reflection and transmission across the seven mirrors, beam expander, and collimator; and an additional 15% loss attributed to the dual-glass interface sealing the etching bath. Any losses from scattering or absorption in the chemical solution weren't measured directly. These stages are summarized in Table 3.2.

Table 3.2 Measured power levels and estimated transmission losses across optical path

Measurement Location	**Power (mW)**	**Loss (%)**
Laser output (setpoint 1 W)	947.5	5
After 7 mirrors + optics	~617	~35 (33 in total)
After chamber glass windows (wafer)	499.8	~20 (12 in total)
Total Loss	–	~50

The laser beam diameter at the wafer surface was measured to be approximately 1.6 cm, verified by laser-sensitive alignment paper and visual inspection. Assuming a circular Gaussian beam profile, the illuminated area was calculated as:

$$A = \pi\left(\frac{d}{2}\right)^2 = \pi\left(\frac{1.6\,\text{cm}}{2}\right)^2 \approx 2.01\,\text{cm}^2 \tag{3.2}$$

Given a final delivered power of 500 mW, the average power density at the wafer surface was estimated as:

$$\frac{P}{A} = \frac{500\,\text{mW}}{2.01\,\text{cm}^2} \approx 249\,\text{mW/cm}^2 \tag{3.3}$$

This uniform optical power distribution over a relatively broad area was essential for achieving consistent and homogeneous nanohole formation. All experiments referenced the 1 W nominal laser output as the standard operating condition, with power delivery losses accounted for post hoc during analysis.

3.13 Experimental Procedure and Wafer Analysis

Following the detailed explanation of the optical setup and chemical etchant formulation, this section outlines the experimental procedure for fabricating inverted nanohole structures on silicon wafers and the methodology used to evaluate their surface characteristics. The goal is to identify optimal process parameters, specifically laser power and exposure time, to yield the most uniform and lowest reflectivity surfaces. Two distinct types of wafers, saw-damaged wafers, and saw-damage-removed wafers were tested under identical conditions to assess the impact of surface preparation on etching outcomes: SD wafers and SDR wafers.

The silicon wafers used in this study were n-type, Czochralski-grown, (100)-oriented single-crystal wafers with a thickness of 250 μm and a resistivity in the range of 1–1.3 $\Omega \cdot$ cm. These specifications were chosen to represent standard photovoltaic-grade substrates and to ensure compatibility with the photochemical etching process.

Each wafer type was subjected to controlled photochemical etching using the SS-INH-PCE setup. The incident laser power and exposure time were varied systematically in preliminary trials to identify the configuration that resulted in uniform, deep nanohole structures with minimal reflectance. The reflectance was measured across the 300–1200 nm wavelength range using a UV-Vis-NIR spectrophotometer equipped with an integrating sphere. In addition to total reflectance, reflection haze, a metric indicating light scattering due to surface texturing, was recorded to assess the degree of light diffusion. Reflection haze (H) quantifies the extent of light scattering caused by surface nanostructures and is defined as:

$$H = \frac{R_{\text{diffuse}}}{R_{\text{total}}} \times 100\% \tag{3.4}$$

where R_{diffuse} and R_{total} represent the diffuse and total reflectance components, respectively, as measured by the spectrophotometer.

The following subsections provide detailed analysis and characterization results for each wafer type. Scanning electron microscopy was used to visualize the etched surfaces post-process. Comparative plots of reflectance and reflection haze are presented to quantify the effectiveness of the surface structuring for both SD and SDR wafers.

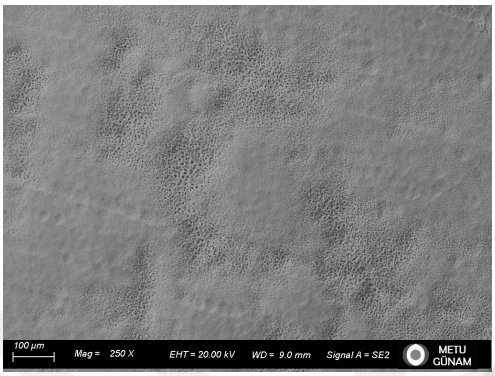
To ensure the results were reliable, each photochemical etching and measurement was repeated three times under the same conditions. The chapter presents the average reflectance values, and standard deviations were included wherever relevant.

3.13.1 Etching of SD Wafers

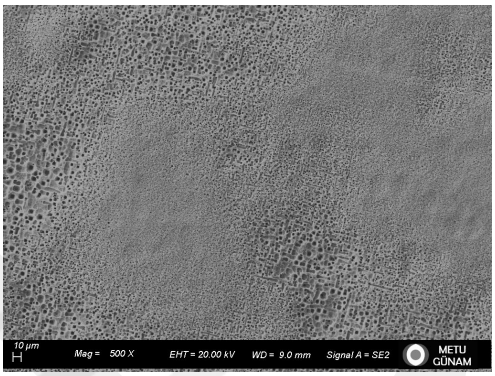
To determine the optimal photochemical etching parameters for SD wafers, a series of tests were conducted by varying two critical variables: laser power and exposure time. The objective was to achieve a uniform and deep nanostructuring with minimized reflectance. During these trials, both SEM and spectral reflectance measurements were used to evaluate the outcomes of different process conditions.

Figure 3.29 provides representative SEM images of the etched SD wafer. These

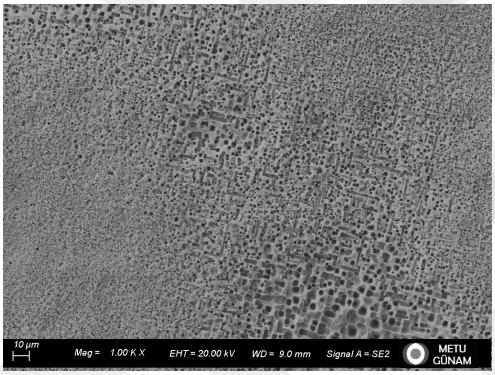
images were captured at magnifications of 250x, 500x, 1000x, and 2000x, respectively. The increasing magnification reveals progressive details of the surface morphology and the distribution of nanoholes induced by the PCE process. The SEM imaging was performed under the following conditions: accelerating voltage (EHT) of 20 kV, working distance (WD) of 8.5 mm, and detection mode using signal A: SE2.



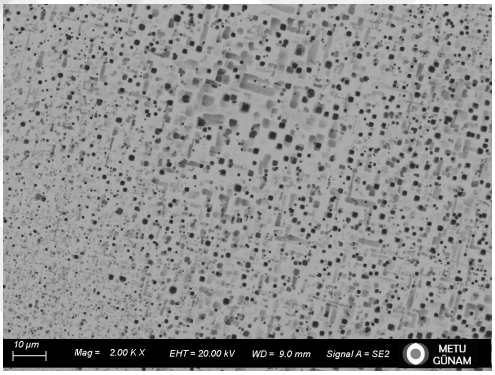
(a) 250x magnification



(b) 500x magnification



(c) 1000x magnification



(d) 2000x magnification

Figure 3.29 SEM images of etched SD wafer surface at different magnifications (EHT: 20 kV, WD: 8.5 mm, Signal A: SE2). Nanoholes can be seen forming across the surface, with increased structural detail visible at higher magnifications.

The SEM micrographs demonstrate the successful formation of inverted nanohole structures across the wafer surface. Overall texturing uniformity is seen at low magnifications, such as 250x and 500x, with a uniform distribution of etched features. Individual nanohole dimensions show slight variations in depth and diameter at higher magnifications (1000x and 2000x). This randomness is typical in optically driven etching processes, especially under ambient conditions without lithographic patterning. Nevertheless, these features also confirm efficient energy coupling and consequent oxidation/dissolution reactions within the etchant medium.

Additionally, Figure 3.30 presents a high-magnification SEM image (25,000x) of an individual nanohole, providing a detailed view of its structure and dimensions. A typical nanohole, such as the one shown here, measures about 3.14 μm wide and 3.03 μm high, presenting a larger-than-average feature than typical nanoholes. The SEM parameters were: EHT = 20.00 kV, WD = 11.5 mm, and Signal A = SE2.

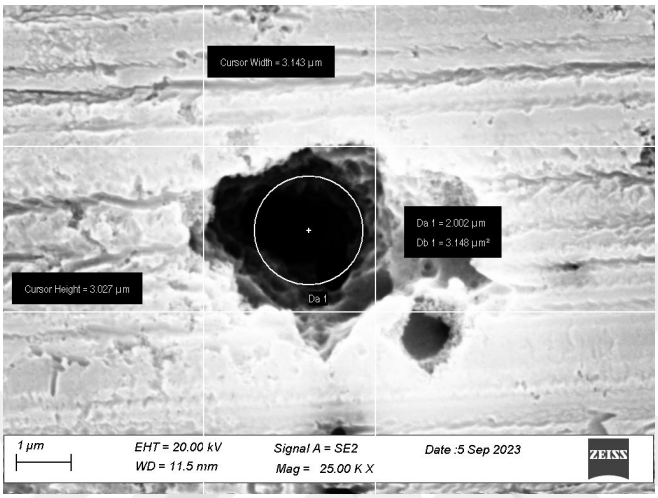


Figure 3.30 High-magnification SEM image (25,000x) showing an individual microhole etched on an SD wafer (EHT: 20.00 kV, WD: 11.5 mm, Signal A: SE2). The nanohole is approximately 3.14 μm wide and 3.03 μm tall.

Larger nanoholes may initially appear advantageous due to their increased surface area and depth, which can potentially enhance light trapping by promoting multiple internal reflections. However, excessively large features can lead to non-uniform surface morphologies and increased defect-related recombination, as illustrated in Figure 3.30. In contrast, overly shallow or sub-micron features, often classified as microholes, tend to exhibit significantly reduced light-trapping efficiency. Given these considerations, it is critical to avoid both extremes in nanohole geometry. Instead, maintaining a balanced and controlled size distribution is essential for achieving optimal optical and electrical performance in photochemically textured silicon surfaces.

3.13.1.1 Reflectivity Measurements of SD Wafers

To optimize laser parameters, the reflectivity of SD wafers was analyzed as a function of laser power and exposure time. Figure 3.31 displays reflectance spectra for SD wafers etched for 15 minutes under varying laser power levels. It was observed that applying

0.5 W resulted in a negligible reduction in reflectance compared to the untreated wafer, while 2 W produced a significant decrease. Higher powers were not tested due to vaporization effects at the etching bath surface, which inhibited etching. Thus, 2 W was selected as the maximum adequate power.

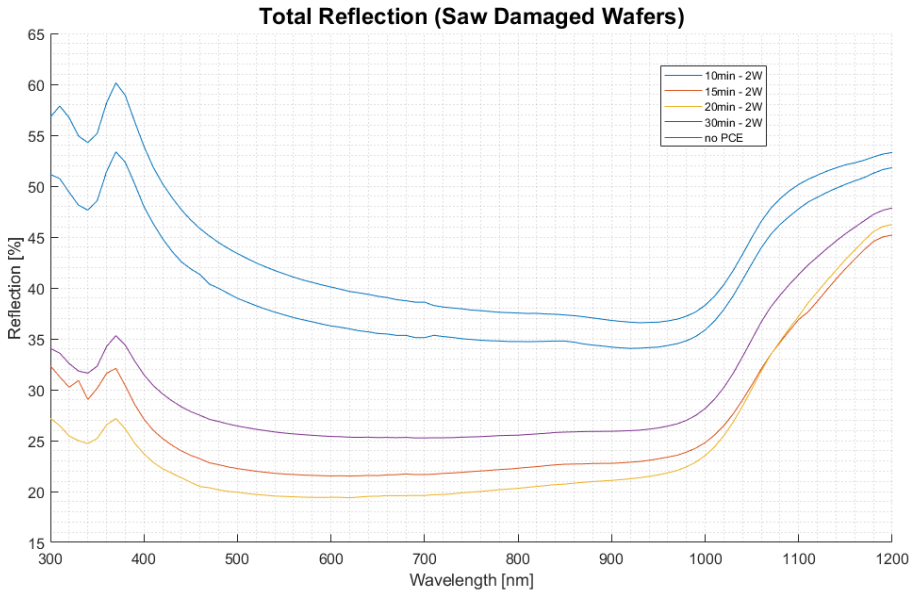


Figure 3.31 Total reflection spectra of SD wafers etched for 15 minutes under different laser power levels. The 2 W condition yielded the most significant reduction in reflectivity.

In Figure 3.32, the impact of exposure time on reflectivity was examined. Keeping the laser power constant at 2 W, wafers were etched for 10, 15, 20, and 30 minutes. The 20-minute etch yielded the lowest reflectance values, indicating that prolonged exposure improves surface texturing.

Figure 3.33 compiles the results of both sets of experiments. The lowest reflectance was achieved with 2 W laser power applied for 20 minutes, confirming this as the optimal etching condition for SD wafers. The spectral data clearly shows that both increasing power and extending time contribute to effective surface nanostructuring.

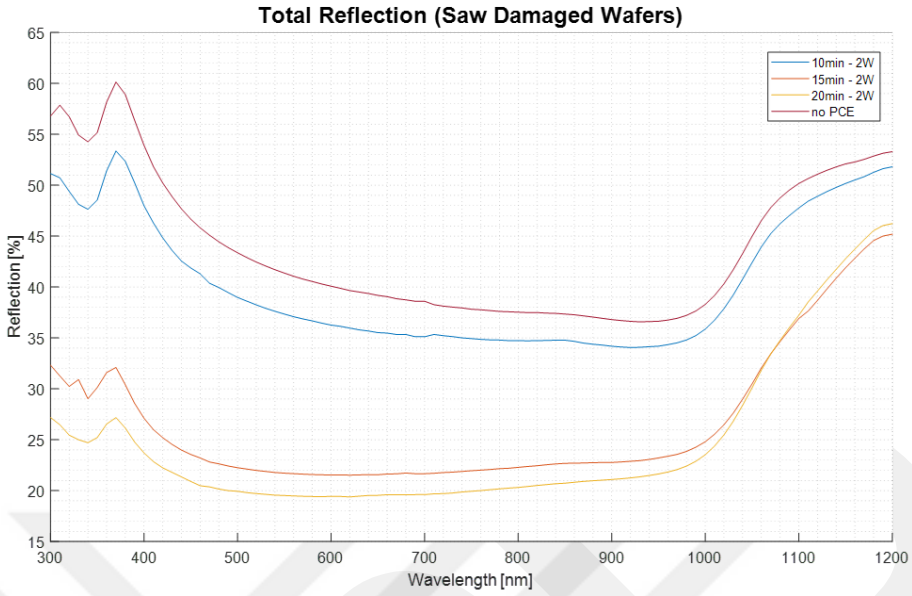


Figure 3.32 Total reflection spectra of SD wafers at a constant 2 W laser power with varying etching durations. A 20-minute exposure resulted in the lowest reflectivity.

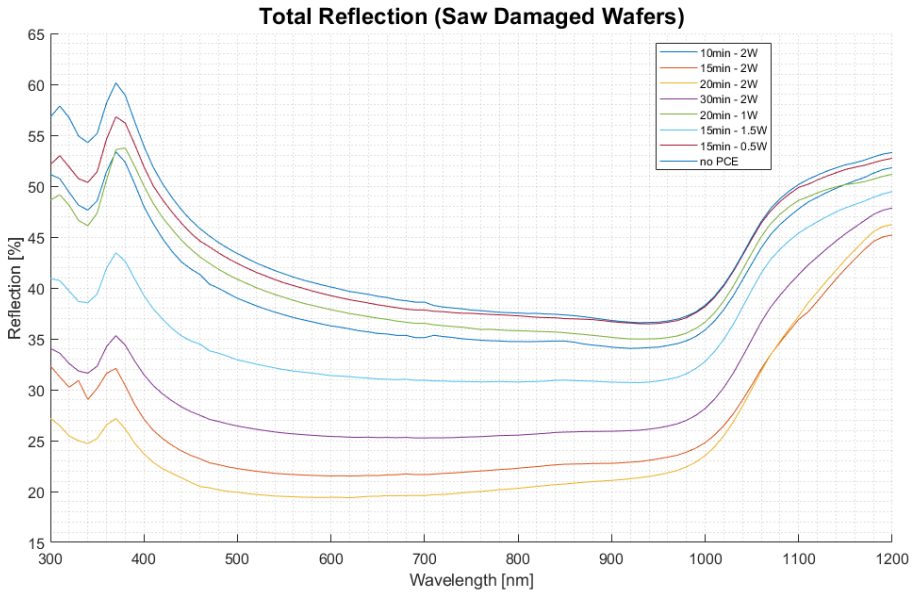


Figure 3.33 Combined reflectance spectra for SD wafers etched at different power levels and exposure durations. The lowest reflectivity was observed for the sample etched at 2 W for 20 minutes.

3.13.1.2 Reflectivity Measurements of SDR Wafers

This subsection will include experimental conditions applied to SDR wafers, representative SEM images after etching, reflectance results, and corresponding haze curves.

Once the optimal power was determined to be 2 W, reflection measurements were conducted only as a function of etching duration for SDR wafers. The goal was to compare how SDR wafers respond to different exposure times when processed at the optimal laser power.

The effect of exposure duration on reflectance was investigated in Figure 3.34. The wafers were etched for 10, 15, and 20 minutes using a constant 2 W laser power. The 20-minute etch gave the lowest reflectance, suggesting that longer exposure improves surface texturing.

This result emphasizes the process sensitivity of SDR wafers and demonstrates that an optimal exposure duration of 15 minutes under 2 W laser power yields the best reflectance suppression.

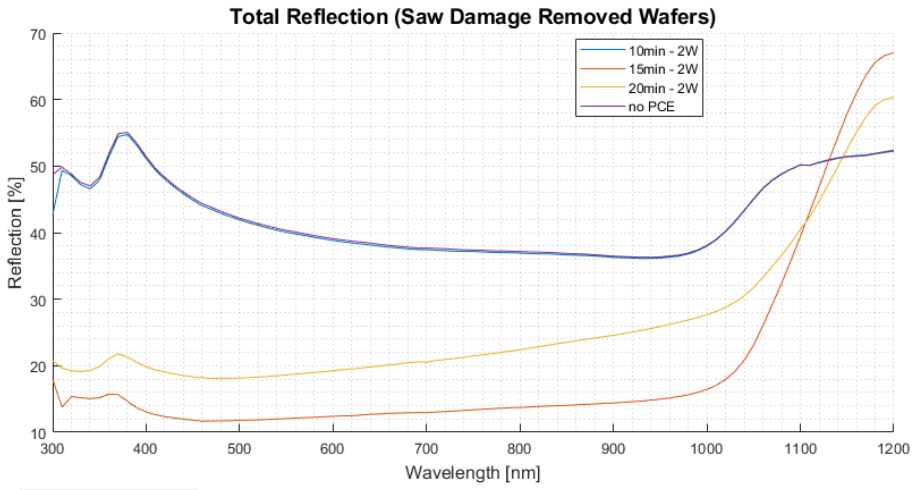


Figure 3.34 Total reflectance of SDR wafers etched for 10, 15, and 20 minutes at 2 W laser power. The 15-minute exposure yielded the lowest reflectance, indicating the optimal etching duration.

The observed increase in total reflectance beyond 1000 nm for the 15-minute and 20-minute etched SDR wafers may be attributed to the diminished absorption efficiency of silicon in the near-infrared region. As the absorption coefficient of crystalline silicon decreases with increasing wavelength, photons in this spectral range are more likely to be reflected rather than absorbed. Additionally, surface nanostructures optimized for visible light trapping may become less effective at longer wavelengths due to scale mismatch, reducing anti-reflective behavior in the NIR regime.

3.13.1.3 Comparison of SD, SDR, and Standard Wafers

To better evaluate the effectiveness of the single-step photochemical etching technique, the total reflectance and reflection haze values of the most optimal SD and SDR wafers were compared with those of a standard unprocessed silicon wafer. The resulting spectra are shown in Figure 3.35 and Figure 3.36.

As seen in Figure 3.35, the unetched standard wafer reflects the most light overall, especially in the visible range where reflectance goes over 50% near 400 nm. In contrast, the SD and SDR wafers etched using the optimized PCE process reflect much less light, showing how well the inverted nanohole structures work to reduce surface reflections. Among them, the SDR wafer etched for 15 minutes at 2 W presents the lowest reflectance, falling below 15% in the visible region and maintaining reduced reflectivity across the entire spectrum. This can be attributed to the smoother initial surface condition of SDR wafers, which enhances the uniformity and depth of nanostructuring, thereby improving light-trapping capabilities. In contrast, while the SD wafer etched for 20 minutes at 2 W also shows substantial improvement, its performance is slightly inferior to that of the SDR wafer due to the presence of initial saw damage interfering with uniform etching.

The reflection haze results, shown in Figure 3.36, further support this conclusion. The SDR wafer exhibits the highest haze values, exceeding 100% in the UV-visible region and remaining significantly elevated across the full spectral range. High haze values indicate increased light scattering, which is desirable for photovoltaic applications as it promotes photon path-length enhancement within the absorber layer. The SD wafer also demonstrates enhanced haze compared to the standard wafer, but the effect is less

pronounced than in the SDR case. This discrepancy again highlights the importance of wafer surface preparation prior to PCE, as the absence of surface defects in SDR wafers leads to more effective nanostructure formation.

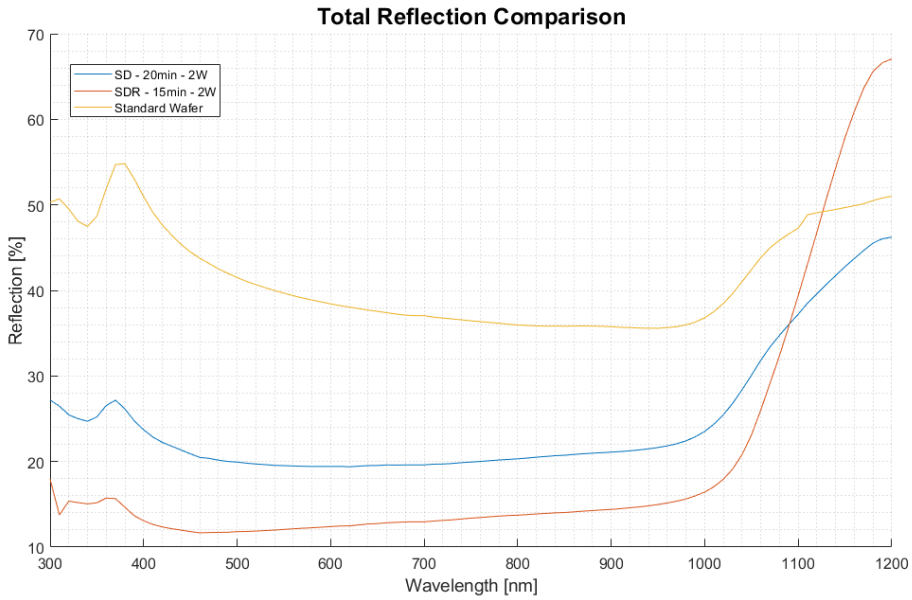


Figure 3.35 Total reflectance spectra of SD (20 min - 2 W), SDR (15 min - 2 W), and standard wafers across the 300–1200 nm wavelength range.

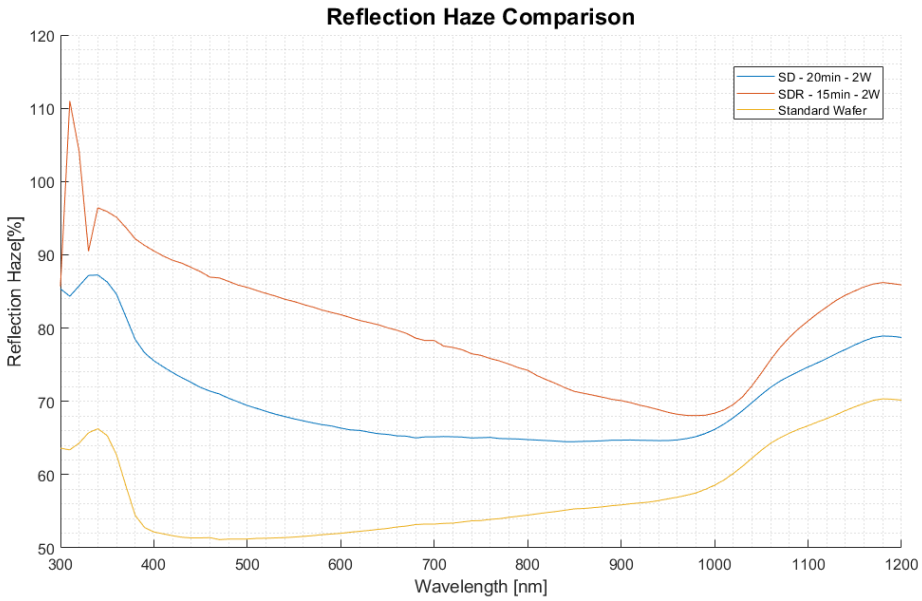


Figure 3.36 Reflection haze comparison of SD, SDR, and standard wafers under optimal etching conditions.

3.14 Discussion of PCE

To assess the efficacy of the single-step inverted nanohole photochemical etching technique, reflectivity measurements were performed using the Bentham PVE 300 UV-Vis-NIR spectrophotometer. These measurements show that the SS-INH-PCE method reduces surface reflectance by forming well-defined inverted nanohole structures on silicon substrates. The acquired spectral data confirm the reliability and industrial viability of the proposed method.

Table 3.3 presents the average total reflectance values obtained for standard (unetched) wafers, saw-damaged wafers subjected to SS-INH-PCE, and saw-damage removed wafers also processed with SS-INH-PCE. The values reflect the mean reflectance across the 300–1200 nm moval and subsequent SS-INH-PCE processes. This reduction is due to a smoother and uniform initial surface condition facilitating consistent nanostructure formation during etching.

Table 3.3 Comparison of average total reflectivity among wafer types

Wafer Type	**Average Reflectivity [%]**
SD (etched)	23.79
SDR (etched)	18.74
Standard (unetched)	41.32

The lowest average reflectivity is 18.74% with the SDR wafer out of all the sample we tested. This reduction is attributed to the smoother and more uniform initial surface condition, which enhances the formation of consistent nanostructures during the etching process.

Although the SD wafer began with greater surface roughness, it still demonstrated a significant improvement, with reflectivity decreasing from 41.32% (unetched) to 23.79% following SS-INH-PCE treatment.

The observed 17.53 percentage point reduction in the SD wafer's reflectivity underscores the robustness of the SS-INH-PCE technique, even in the presence of mechanical surface imperfections. This finding suggests that the conventional SDR procedure may no longer be a necessary prerequisite for effective nanostructuring.

This conclusion has valuable practice consequences. Most SDR processes

use aggressive chemical or mechanical treatments that are both time and resource-demanding and present health and safety risks since hazardous materials are involved. The operation of overriding the SDR step has the advantages below:

- **Less process steps:** Eliminates SDR, AR coating, silver pasting, and firing. Higher cycle time and productivity.
- **Cost efficiency:** Fewer consumables and special equipment are used, resulting in lower manufacturing costs.
- **Enhanced safety:** Avoids the fear of being exposed to harmful corrosive chemicals in SDR.
- **Scalability:** Streamlined processing can be scaled up for large manufacturing runs.

Consequently, the SS-INH-PCE technique not only matches the optical performance of methods requiring SDR but also surpasses them in terms of operational simplicity, economic viability, and process sustainability. Its effectiveness on both SD and SDR wafers positions it as a promising universal surface texturing approach for next-generation silicon photovoltaics.

3.15 Single-Step Inverted Nanohole Photochemical Etching

The experiments conducted in the previous chapter were primarily focused on a localized surface area of approximately 2 cm^2, allowing detailed analysis of nanohole formation, reflectivity, and process optimization. However, for practical photovoltaic applications, the photochemically textured region must be extended to cover an entire standard-sized wafer. This section explores the feasibility of scaling the SS-INH-PCE process from small-area applications to full-wafer coverage (256 cm^2) using optical beam expansion strategies.

To achieve full-surface processing, significant adaptations to the optical setup were implemented. The primary challenge was to expand the laser beam diameter from its initial size (1.6 cm) to approximately 4 cm and eventually to 16 cm. As illustrated in

Figure 3.37, the optical path was modified by increasing the distance between the beam expander and the collimator. This allowed the generation of broader beam profiles, with final spot diameters tailored to different target areas.

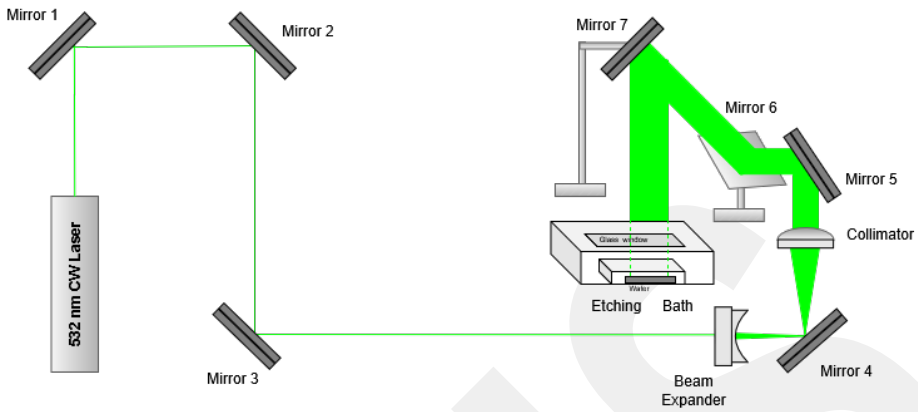
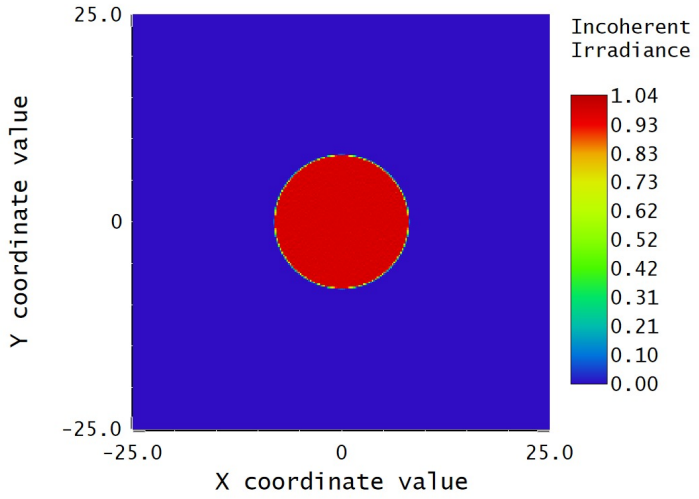


Figure 3.37 Proposed optical system modification for full-wafer SS-INH-PCE. The beam expander is repositioned to allow a larger beam diameter, enabling coverage of a 16 cm × 16 cm wafer.

Two optical configurations were modeled in Ansys Zemax OpticStudio 2023 R1. The first configuration, with a 2 W CW laser source, produced a 1.6 cm diameter spot. The second, using a 6.5 W laser, yielded a 4 cm diameter spot, corresponding to a 2.5-fold increase in diameter and a 6.25-fold increase in area:

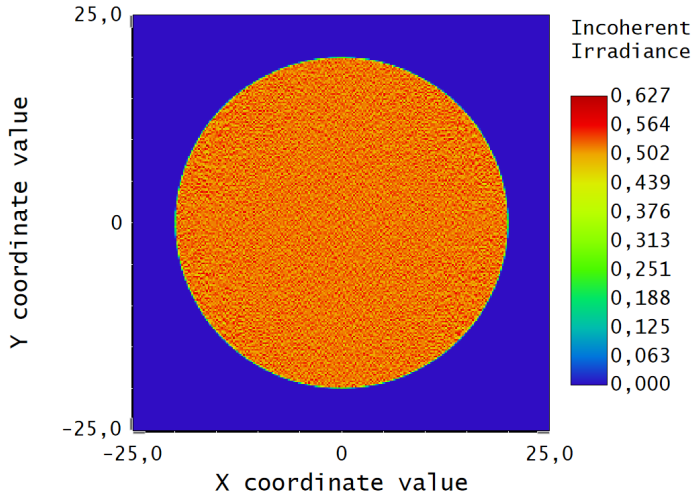
$$A = \pi\left(\frac{d}{2}\right)^2 = \pi\left(\frac{4\,\text{cm}}{2}\right)^2 \approx 12.57\,\text{cm}^2 \tag{3.5}$$



Detector Image: Incoherent Irradiance

Optical Model of PCE Setup with 2W Laser Power 30/05/2025 Detector 5, NSCG Surface 1: Field 1 Size 50.000 W X 50.000 H Millimeters, Pixels 250 W X 250 H, Total Hits = 1000000 Peak Irradiance : 1.0387E+00 Watts/cm^2 Total Power : 1.9785E+00 Watts	Zemax Ansys Zemax OpticStudio 2024 R1.00 GV_optical_model_2W-NONSEQ.zmx Configuration 1 of 1

Figure 3.38 Simulated irradiance profile for 1.6 cm diameter spot using 2 W laser.



Detector Image: Incoherent Irradiance

Optical Model for Increased Spot Size with 6.5W Laser Power 29.05.2025 Detector 5, NSCG Surface 1: Field 1 Size 50,000 W X 50,000 H Millimeters, Pixels 250 W X 250 H, Total Hits = 1000000 Peak Irradiance : 6,2695E-01 Watts/cm^2 Total Power : 6,4302E+00 Watts	Zemax Ansys Zemax OpticStudio 2023 R1.00 GV_optical_model_6.5W-NONSEQ.zmx Configuration 1 of 1

Figure 3.39 Simulated irradiance profile for 4 cm diameter spot using 6.5 W laser.

Irradiance Uniformity Across Beam Cross-Section

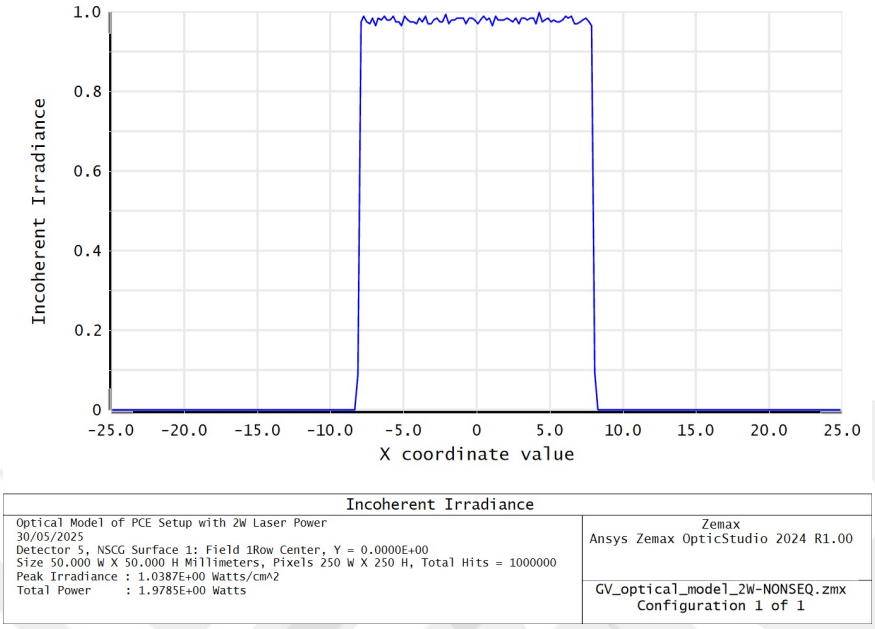


Figure 3.40 Incoherent irradiance profile along the X-axis for the 2 W, 1.6 cm spot configuration. The irradiance is sharply bounded and highly uniform across the beam cross-section.

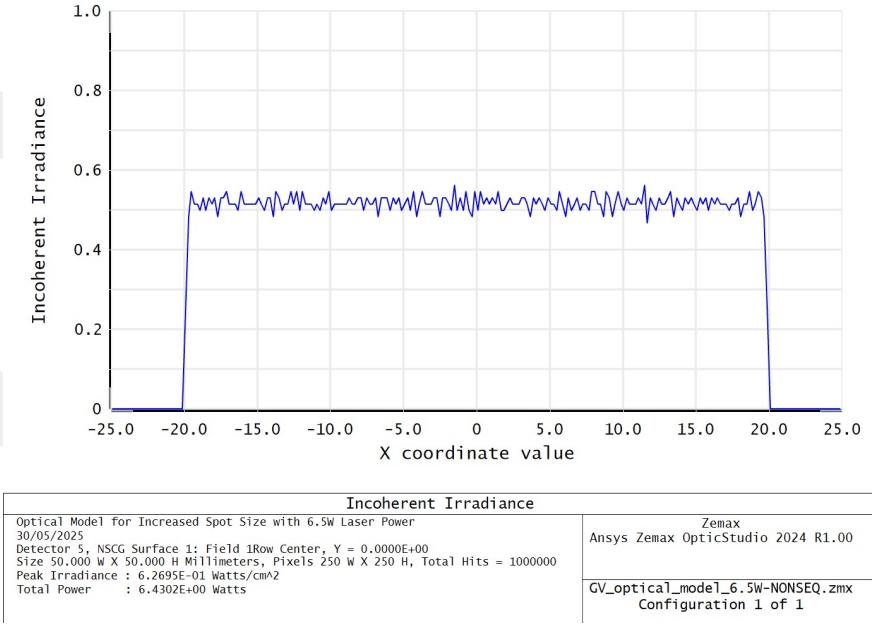


Figure 3.41 Incoherent irradiance profile along the x-axis for the 6.5 W, 4 cm spot configuration. Even though the spot size was larger, the laser's energy stayed evenly spread across the target area.

To validate the spatial uniformity of irradiance across the beam footprint, line profile plots were extracted from Zemax simulations for both optical configurations. These plots represent the incoherent irradiance distribution along the horizontal (X) axis through the center of the beam spot.

Figures 3.40 and 3.41 show that both beam setups produce a flat and even irradiance profile, meaning the laser power spreads out uniformly across the active area. This flat-topped distribution is crucial for achieving homogeneous photochemical etching across the entire illuminated area, minimizing spatial variation in nanohole dimensions and surface reflectance.

These results confirm that the optical system not only enables spot expansion but also maintains the irradiance uniformity required for effective and consistent SS-INH-PCE processing.

Despite the lower irradiance resulting from beam expansion, the 6.5,W laser power was experimentally sufficient to successfully perform PCE over a 4 $\times$4cm^2 area, validating the effectiveness of the proposed optical configuration.

Irradiance Calculation for 4 $\times$ 4 cm^2 Area

$$P = 6.5\,\text{W} \tag{3.6}$$

$$A = 4\,\text{cm} \times 4\,\text{cm} = 16\,\text{cm}^2 \tag{3.7}$$

$$E = \frac{P}{A} = \frac{6.5\,\text{W}}{16\,\text{cm}^2} = 0.40625\,\text{W/cm}^2 \tag{3.8}$$

Considering an estimated 50% optical loss, the effective irradiance at the wafer becomes:

$$E_{\text{eff}} = 0.40625\,\text{W/cm}^2 \times 0.5 = 0.203\,\text{W/cm}^2 \tag{3.9}$$

Under these conditions, PCE was achieved by exposing each 4 $\times$4cm^2 quadrant for 30 minutes. This process was repeated 16 times to ensure full-area coverage across the

16 ×16cm^2 wafer, aiming for consistent treatment across all regions.

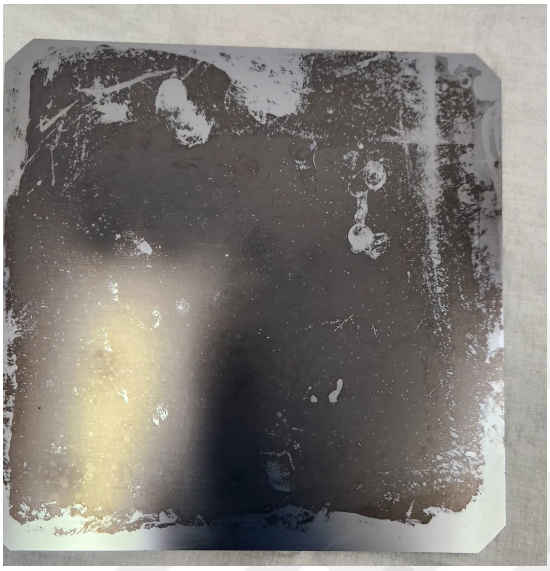


Figure 3.42 Final surface appearance of the 16 × 16 cm^2 wafer after completing 16-step sequential PCE.

Surface Comparison of Processed Wafers

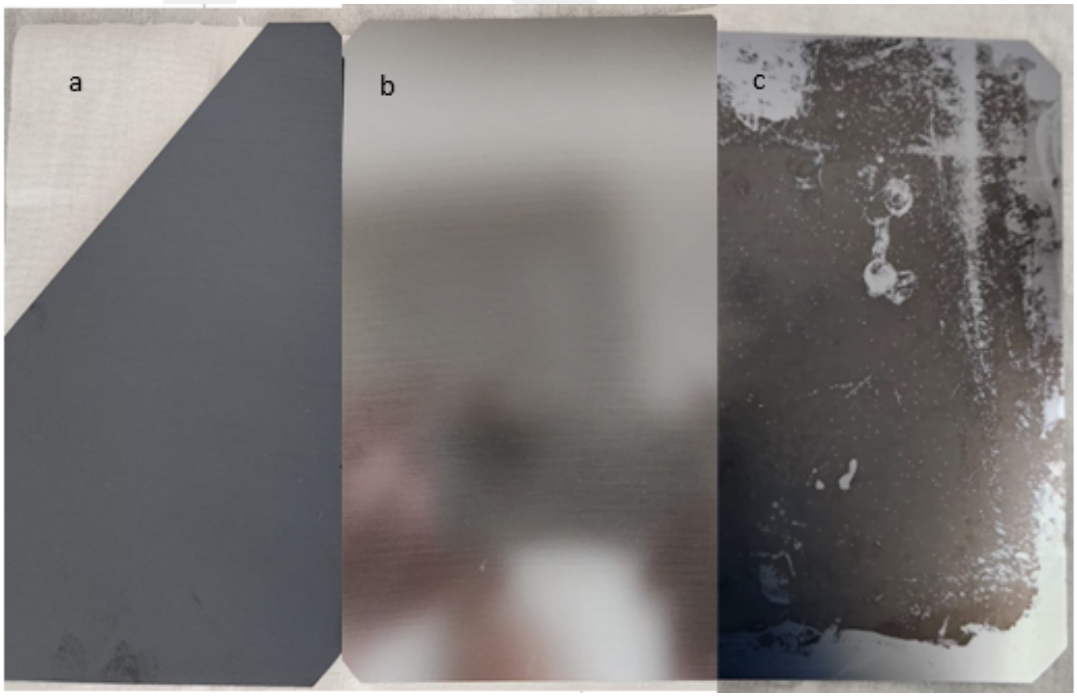


Figure 3.43 Visual comparison of different wafer surfaces: (a) Conventionally textured wafer, (b) SDR wafer, (c) Wafer processed via the SS-INH-PCE method.

Figure 3.43 presents a visual comparison of three different silicon wafer surfaces evaluated in this study. Image (a) displays a conventionally textured wafer produced via standard alkaline etching, commonly used in industrial photovoltaic applications. Image (b) shows a SDR wafer, chemically treated to smooth the surface but lacking nanostructures for enhanced light trapping. Image (c), by contrast, depicts a wafer etched using the proposed SS-INH-PCE method. Its distinctly darker appearance indicates significantly lower surface reflectivity—an optical trait reminiscent of black silicon. However, unlike black silicon, which typically requires complex and costly fabrication steps such as femtosecond laser processing or reactive ion etching, the SS-INH-PCE approach offers a simpler, scalable, and low-cost alternative while achieving comparable anti-reflective characteristics.

Irradiance Estimation for $16 \times 16\ \mathrm{cm}^2$ Spot

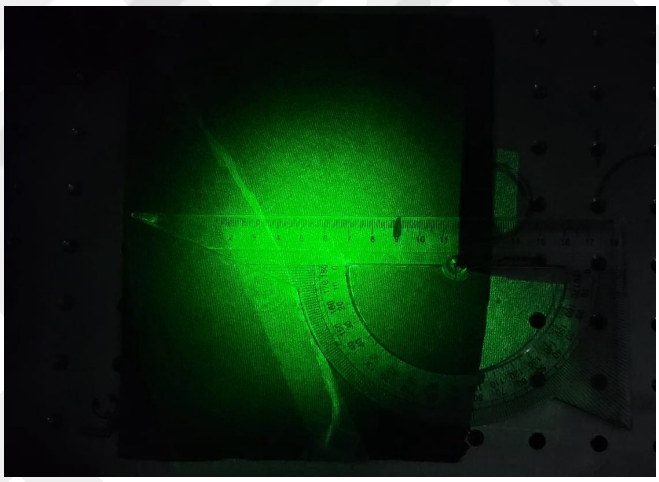


Figure 3.44 Laser beam expanded to approximately 16 cm diameter for full-wafer exposure.

To explore single-shot etching, the beam diameter was further increased to 16 cm (covering $256\ \mathrm{cm}^2$) by repositioning the beam expander. However, this drastically reduced the irradiance:

$$A = 16\,\mathrm{cm} \times 16\,\mathrm{cm} = 256\,\mathrm{cm}^2 \tag{3.10}$$

$$E = \frac{P}{A} = \frac{6.5\,\text{W}}{256\,\text{cm}^2} \approx 0.0254\,\text{W/cm}^2 \tag{3.11}$$

This irradiance value is an order of magnitude lower than the minimum required for effective PCE. As a result, no etching took place, highlighting just how important it is to maintain enough power density to trigger the chemical reaction with light.

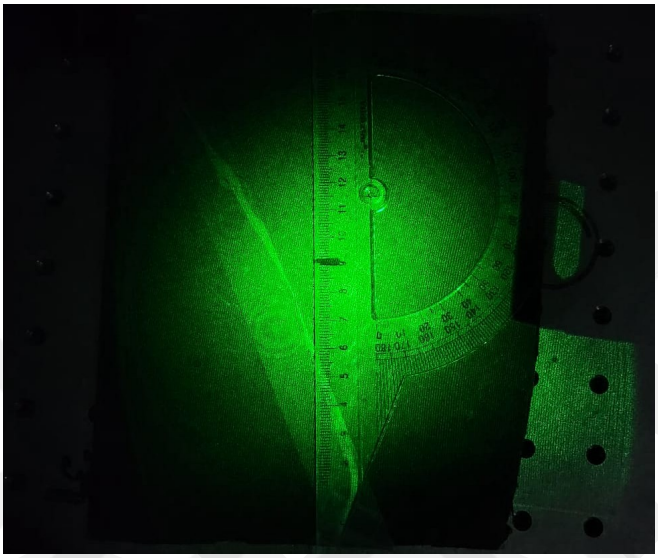


Figure 3.45 Laser spot projected onto the entire wafer surface.

Challenges of HF Evaporation and Condensation During Laser-Assisted Photochemical Etching

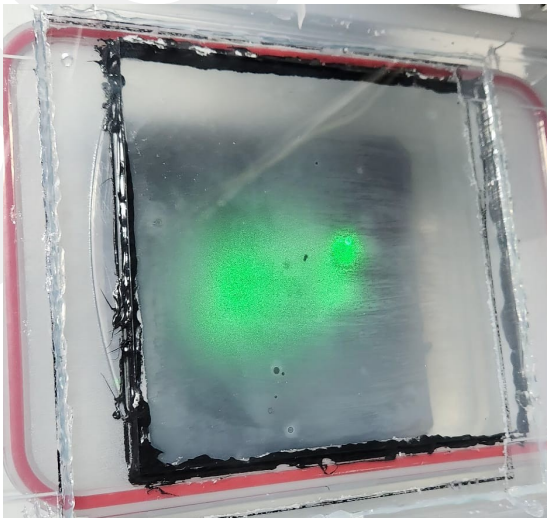


Figure 3.46 HF vapor condensing on the glass surface, obstructing the laser path.

One of the most critical challenges encountered in this study is the mitigation of HF condensation and evaporation during the photochemical etching process. Given that HF has a low condensation point (approximately 20°C), the high-power continuous-wave laser used for localized etching significantly heats the chemical mixture, making evaporation and subsequent condensation inevitable. As illustrated in Figure 3.46, HF condensation on the inner surface of the glass chamber scatters or absorbs the laser beam, thereby preventing full transmission to the silicon wafer. Moreover, the condensed HF gradually etches the glass interface, compromising both the structural integrity and repeatability of the experimental setup. An initial attempt to address this issue using a heated resistance wire to suppress condensation proved ineffective, emphasizing the need for a more robust thermal management or chamber design solution to ensure consistent and uninterrupted laser delivery throughout the etching process.

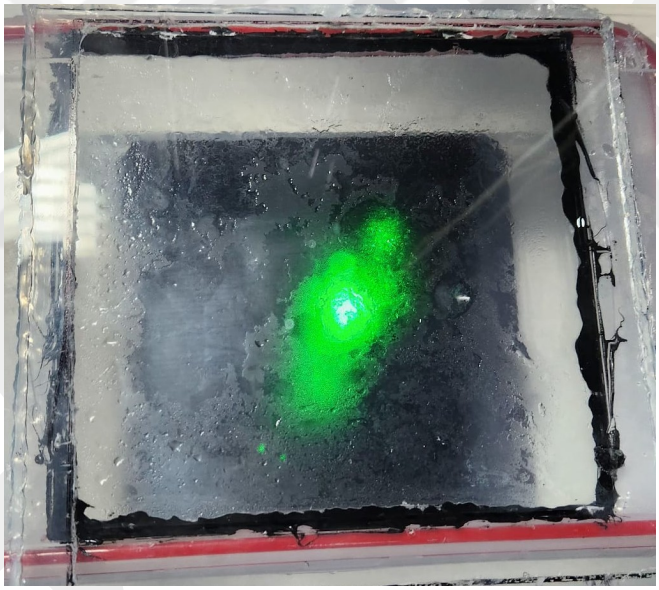


Figure 3.47 Evaporation-induced HF mist formation inside the chamber.

To minimize the presence of HF vapor and ensure unobstructed laser transmission to the wafer surface, a cooling fan was employed during the tests. Additionally, to maintain repeatability, the glass cover positioned above the etching bath was replaced prior to each experiment due to HF-induced degradation. However, when the etching process is carried out for extended durations, similar condensation-related issues are likely to reoccur. Therefore, in a production setting, the integration of a dedicated

thermal bath for temperature regulation becomes essential to ensure both process stability and equipment longevity.

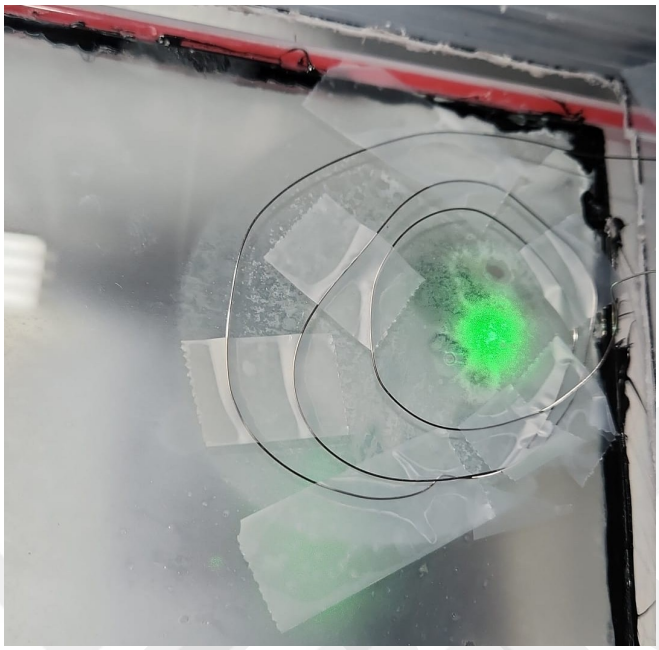


Figure 3.48 Heated resistance wire placed above the reaction chamber in an attempt to prevent condensation.

3.16 Future Prospect

To further enhance the performance and scalability of the SS-INH-PCE process, the most immediate strategy involves increasing the available laser power. As shown in previous sections, the irradiance level is inversely proportional to the illuminated area. Therefore, achieving single-pass etching on larger substrates such as a 16×16 cm^2 wafer requires significantly higher laser output. Assuming a minimum required irradiance of approximately 0.2 W/cm^2 (based on effective etching in the 4×4 cm^2 region), the theoretical power required to uniformly irradiate a 256 cm^2 area can be estimated as:

$$P = E \times A = 0.2\,\text{W/cm}^2 \times 256\,\text{cm}^2 = 51.2\,\text{W} \tag{3.12}$$

This calculation highlights the necessity of employing laser sources exceeding 50 W to feasibly implement single-shot full-wafer SS-INH-PCE under current optical

conditions.

Another improvement pathway lies in minimizing optical losses within the beam delivery system. In the current setup, total transmission efficiency is limited by reflection and absorption losses at multiple optical interfaces. Replacing standard dielectric mirrors with high-reflectivity, laser-grade coatings (e.g., $R > 99.8\%$ at 532 nm) could substantially reduce power attenuation. Likewise, using better anti-reflective coatings on the lenses and simplifying the optical setup by reducing the number of components would help more light reach the wafer. These improvements would boost the power delivered to the wafer without needing a stronger laser, making the process more workable even with lower-power systems.

In addition to optical and power-related improvements, the issue of HF vapor condensation remains a critical obstacle for long-duration etching. To address this, the implementation of a closed-loop thermal bath system is recommended in future designs. Such a system would actively regulate the temperature of the etching environment, suppressing HF evaporation and condensation near the laser path. This solution is essential for ensuring stable long-term operation and reproducibility, particularly in industrial-scale applications.

Beyond optical characterization, a crucial future objective is to fabricate complete solar cell from the etched wafers and evaluate their electrical performance. Assessing parameters such as open-circuit voltage, short-circuit current, and overall conversion efficiency would provide comprehensive insight into the functional advantages of the SS-INH-PCE technique. Demonstrating electrical benefits in addition to optical enhancements would significantly elevate the technological impact of this work.

CHAPTER 4
CONCLUSION

This thesis presented the development, implementation, and validation of a SS-INH-PCE technique for crystalline silicon wafers. The SS-INH-PCE method integrates continuous-wave laser irradiation with a chemically tailored etchant solution composed of HF, H_2O_2, and DI water, enabling lithography-free nanostructuring under ambient laboratory conditions. The optical and chemical setup was systematically designed to facilitate stable and reproducible etching of silicon surfaces through localized photo-induced oxidation and wet chemical dissolution mechanisms.

The SS-INH-PCE process offers several key advantages over conventional texturing and etching methods. Its operation at room temperature and atmospheric pressure eliminates the need for cleanroom infrastructure, vacuum systems, or high-temperature processing. The method's simplicity allows low-cost prototyping and opens new avenues for scalable surface modification in photovoltaic, optoelectronic, and MEMS applications. The chemical formulation of the etching solution was optimized by balancing oxidation potential and etch aggressiveness to obtain well-defined inverted nanohole structures with uniform morphology. The method significantly reduces the number of processing steps required for device fabrication. Specifically, it eliminates the need for conventional steps such as SDR, AR coating, silver pasting, and firing.

Beyond the localized fabrication of nanostructures, the SS-INH-PCE technique was further examined for its scalability to full-wafer processing. To achieve this, optical system modifications were designed to increase the beam diameter and enable uniform illumination over standard 16 cm $\times$ 16 cm wafers. However, due to the nonlinear relationship between area and irradiance, directly expanding the beam without increasing the laser power led to a significant reduction in power density, which fell below the threshold required for effective etching. To work around this limitation, the wafer was divided into sixteen separate 4 cm $\times$ 4 cm sections, and each

one was processed one at a time by repositioning the laser beam. This step-by-step method made it possible to get enough irradiance using the available 6.5 W laser, allowing full wafer coverage without needing a much more powerful source.

This approach offers a practical pathway for scaling the SS-INH-PCE process using existing laboratory equipment. It demonstrates that through precise beam control and exposure planning, large-area nanostructuring is feasible even under moderate power conditions. These findings position SS-INH-PCE as a flexible and scalable method suitable for integration into industrial solar cell manufacturing lines, particularly where cost-efficiency and equipment simplicity are critical.

From a technical perspective, the SS-INH-PCE approach aligns well with recent wafer-level texturing and light management trends. Inverted nanohole formation increases light scattering and absorption, allowing efficiency gains in silicon solar cells. Furthermore, the process automatically removes surface oxides and native defects during etching without any pre-treatment steps. Thus, this lowers chemical use and processing time and increases environmental safety, which is a critical issue in sustainable manufacturing frameworks.

The most important result of this work is that the saw damage removal step could be eliminated, which normally involves mechanical polishing or aggressive alkaline etching. Demonstrating equivalent or better optical performance on SD wafers, the SS-INH-PCE method can shorten the manufacturing sequence, increase throughput, and reduce operation hazards. While this thesis has primarily addressed optical performance metrics, future studies should explore the electrical behavior of solar cells fabricated from SS-INH-PCE-treated wafers, particularly focusing on surface passivation quality and carrier lifetime.

Despite the promising results, certain challenges remain. Uniformity across large areas, edge effects near wafer boundaries, and laser power losses due to beam expansion must be addressed through advanced beam-shaping optics and automated scanning systems. Additionally, real-time etch depth and surface morphology monitoring could improve process control and reproducibility. Including such feedback mechanisms, possibly via inline optical metrology, further improves the reliability of the method in industrial contexts.

To conclude, this work establishes the SS-INH-PCE process as a strong, cost-effective, and scalable nanostructuring technique for crystalline silicon wafers. In addition to its ambient operational conditions and minimal equipment requirements, the method achieves an average reflectivity reduction of 17.5% on saw-damaged wafers, positioning it as a strong candidate for next-generation surface engineering approaches in photovoltaics and beyond. Future work will expand its applicability, refine optical alignment for large-area processing, and evaluate its impact on complete device performance.

REFERENCES

[1] J.T. Fourkas, J. Gao, Z. Han, H. Liu, B. Marmiroli, M.J. Naughton, and Y. Zheng, "Grand challenges in nanofabrication: There remains plenty of room at the bottom," *Frontiers in Nanotechnology*, vol. 3, p. 700849, 2021.

[2] A. Machín and F. Márquez, "Advancements in photovoltaic cell materials: Silicon, organic, and perovskite solar cells," *Materials*, vol. 17, no. 5, p. 1165, 2024.

[3] M. Hammerschmidt, "Optical simulation of complex nanostructured solar cells with a reduced basis method," PhD thesis, Freie Universität Berlin, Berlin, Germany, 2016.

[4] M. Nandipati, O. Fatoki, and S. Desai, "Bridging nanomanufacturing and artificial intelligence—a comprehensive review," *Materials*, vol. 17, no. 7, p. 1621, 2024.

[5] A. Mavrokefalos, S.E. Han, S. Yerci, M.S. Branham, and G. Chen, "Efficient light trapping in inverted nanopyramid thin crystalline silicon membranes for solar cell applications," *Nano Letters*, vol. 12, no. 6, pp. 2792–2796, 2012.

[6] V.A. Popovich, M. Janssen, I.J. Bennett, and I.M. Richardson, "Breakage issues in silicon solar wafers and cells," *Photovoltaics International*, vol. 12, pp. 49–57, 2011, may.

[7] H. Riemann and A. Luedge, "Floating zone crystal growth," in *Crystal Growth of Si for Solar Cells*. Berlin, Heidelberg: Springer Berlin Heidelberg, 2009, pp. 41–53.

[8] N. Werner, *Analysis and automation of the crucible-free Floating Zone (FZ) growth of silicon crystals*. Berlin, Germany: epubli GmbH, 2014.

[9] J.M. Kim and Y.K. Kim, "Saw-damage-induced structural defects on the surface of silicon crystals," *Journal of The Electrochemical Society*, vol. 152, no. 3, p. G189, 2005.

[10] R.K. Kang, Y.F. Zeng, S. Gao, Z.G. Dong, and D.M. Guo, "Surface layer damage of silicon wafers sliced by wire saw process," *Advanced Materials Research*, vol. 797, pp. 685–690, 2013.

[11] Z. Li, S. Gao, R. Kang, H. Li, and X. Guo, "A comparative study of lapping and grinding induced surface/subsurface damage of silicon wafers and corresponding polishing efficiency," *International Journal of Abrasive Technology*, vol. 10, no. 2, pp. 122–133, 2020.

[12] J. Bhardwaj, H. Ashraf, and A. McQuarrie, "Dry silicon etching for mems," in *Proc. Third International Symposium on Microstructures and Microfabricated Systems*, May 1997, pp. 118–130.

[13] M.J. Madou, *Fundamentals of microfabrication and nanotechnology*. Boca Raton, FL, USA: CRC Press, 2012, pp. 53–87.

[14] B. Liu, "Three-dimensional photonic devices and circuits," Ph.D. dissertation, University of California, Santa Barbara, Santa Barbara, CA, USA, March 2000.

[15] G.W. Neudeck and R.F. Pierret, *Introduction to microelectronic fabrication*. Upper Saddle River, NJ, USA: Prentice Hall, 2002, pp. 17–40.

[16] V. Karanassios and G. Mew, "Anisotropic wet chemical etching of si for chemical analysis applications," *Sensors and Materials*, vol. 9, pp. 395–416, 1997.

[17] B. Ziaie, A. Baldi, and M.Z. Atashbar, "Introduction to micro-/nanofabrication," in *Springer Handbook of Nanotechnology*, 2010, pp. 231–269.

[18] R.J. Gasvoda, Z. Zhang, S. Wang, E.A. Hudson, and S. Agarwal, "Etch selectivity during plasma-assisted etching of sio2 and sinx: Transitioning from reactive ion etching to atomic layer etching," *Journal of Vacuum Science & Technology A*, vol. 38, no. 5, 2020.

[19] V.M. Donnelly and A. Kornblit, "Plasma etching: Yesterday, today, and tomorrow," *Journal of Vacuum Science & Technology A*, vol. 31, no. 5, 2013.

[20] R.M. Pinto, V. Gund, C. Calaza, K.K. Nagaraja, and K.B. Vinayakumar, "Piezoelectric aluminum nitride thin-films: A review of wet and dry etching techniques," *Microelectronic Engineering*, vol. 257, p. 111753, 2022.

[21] M. Huff, "Recent advances in reactive ion etching and applications of high-aspect-ratio microfabrication," *Micromachines*, vol. 12, no. 8, p. 991, 2021.

[22] H. Jansen, H. Gardeniers, M. de Boer, M. Elwenspoek, and J. Fluitman, "A survey on the reactive ion etching of silicon in microtechnology," *Journal of Micromechanics and Microengineering*, vol. 6, no. 1, p. 14, 1996.

[23] H.H. Wieder, “Ion-beam milling of silicon carbide epitaxial layers,” California Univ., San Diego Report, Tech. Rep., 1982.

[24] T.V. Vishnu, P. Gupta, P. Malhotra, L. Vig, and G. Shroff, “Recurrent neural networks for online remaining useful life estimation in ion mill etching system,” in *Proceedings of the Annual Conference of the PHM Society*, vol. 22, Philadelphia, PA, USA, September 2018.

[25] C. Cardinaud, M.C. Peignon, and P.Y. Tessier, “Plasma etching: principles, mechanisms, application to micro-and nano-technologies,” *Applied Surface Science*, vol. 164, no. 1–4, p. 72–83, 2000.

[26] K.W. Kolasinski, “The mechanism of si etching in fluoride solutions,” *Physical Chemistry Chemical Physics*, vol. 5, no. 6, pp. 1270–1278, 2003.

[27] G.S. Higashi, Y.J. Chabal, G.W. Trucks, and K. Raghavachari, “N/a,” *Applied Physics Letters*, vol. 56, p. 656, 1990.

[28] A. Wagner, “Koh si wet etch review,” North Dakota State University, Technical Report, 2004, pp. 1–14.

[29] B. Bhushan, Ed., *Springer handbook of nanotechnology*, 3rd ed. Berlin, Germany: Springer, 2017.

[30] J. Bonse and J. Krüger, “Pulse number dependence of laser-induced periodic surface structures for femtosecond laser irradiation of silicon,” *Journal of Applied Physics*, vol. 108, no. 3, 2010.

[31] X. Li, K. Tao, H. Ge, D. Zhang, Z. Gao, R. Jia, and X. Liu, “Improvement of saw damage removal to fabricate uniform black silicon nanostructure on large-area multi–crystalline silicon wafers,” *Solar Energy*, vol. 204, pp. 577–584, 2020.

[32] X. Li, R.R. Rutenbar, and R.D. Blanton, “Virtual probe: A statistically optimal framework for minimum-cost silicon characterization of nanoscale integrated circuits,” in *Proceedings of the 2009 International Conference on Computer-Aided Design*, November 2009, pp. 433–440.

[33] R. Jenkins and R.L. Snyder, *Introduction to X-ray powder diffractometry*. New York: Wiley, 1996, vol. 138.

[34] J.I. Goldstein, D.E. Newbury, P. Echlin, D.C. Joy, C.E. Lyman, E. Lifshin, and J.R. Michael, “Special topics in electron beam x-ray microanalysis,” in *Scanning Electron Microscopy and X-ray Microanalysis: Third Edition*, 2003,

pp. 453–536.

[35] D.B. Williams and C.B. Carter, *The transmission electron microscope*, 2nd ed. Boston, MA, USA: Springer US, 2009, pp. 3–22.

[36] R. García and R. Perez, "Dynamic atomic force microscopy methods," *Surface Science Reports*, vol. 47, no. 6–8, pp. 197–301, 2002.

[37] H.A. Macleod, *Thin-film optical filters*, 4th ed. Boca Raton, FL, USA: CRC Press, 2010.

[38] H. Höffler, F. Schindler, A. Brand, D. Herrmann, R. Eberle, R. Post, and M.C. Schubert, "Review and recent development in combining photoluminescence-and electroluminescence-imaging with carrier lifetime measurements via modulated photoluminescence at variable temperatures," in *Proceedings of the 37th European PV Solar Energy Conference and Exhibition*, vol. 7, September 2020, p. 11.

[39] A. Cuevas, M.J. Kerr, and J. Schmidt, "Passivation of crystalline silicon using silicon nitride," in *3rd World Conference on Photovoltaic Energy Conversion*, vol. 1. IEEE, May 2003, pp. 913–918.

[40] P. Donato, F. Cacciola, P.Q. Tranchida, P. Dugo, and L. Mondello, "Mass spectrometry detection in comprehensive liquid chromatography: basic concepts, instrumental aspects, applications and trends," *Mass Spectrometry Reviews*, vol. 31, no. 5, pp. 523–559, 2012.

[41] P. Chakraborty, "Secondary ion mass spectrometry for quantitative surface and in-depth analysis of materials," *Pramana*, vol. 50, pp. 617–640, 1998.

[42] J. Matthew, "Surface analysis by auger and x-ray photoelectron spectroscopy. d. briggs and j.t. grant (eds)." 2004, iMPublications, Chichester, UK and SurfaceSpectra, Manchester, UK, 2003. 900 pp., ISBN 1-901019-04-7.

[43] D.K. Schroder, *Semiconductor material and device characterization*, 3rd ed. Hoboken, NJ, USA: John Wiley & Sons, 2015.

[44] F.J. Ma, G.G. Samudra, M. Peters, A.G. Aberle, F. Werner, J. Schmidt, and B. Hoex, "Advanced modeling of the effective minority carrier lifetime of passivated crystalline silicon wafers," *Journal of Applied Physics*, vol. 112, no. 5, 2012.

[45] M.A. Green, *Solar cells: Operating principles, technology, and system*

applications. Englewood Cliffs, NJ, USA: Prentice-Hall, 1982.

[46] S.A. Campbell, *The science and engineering of microelectronic fabrication*. New York, NY, USA: Oxford University Press, 2001.

[47] S.M. Sze and K.K. Ng, *LEDs and lasers*, 3rd ed. Hoboken, NJ, USA: Wiley-Interscience, 2006, pp. 789–820.

[48] P.E. Hill and S. D., "Semiconductor devices," *KSU Distinguished Course Repository*, vol. 2, no. 2, p. 2, 2023.

[49] E.H. Rhoderick, "Metal-semiconductor contacts," *IEE Proceedings I (Solid-State and Electron Devices)*, vol. 129, no. 1, 1982.

[50] R.T. Tung, "The physics and chemistry of the schottky barrier height," *Applied Physics Reviews*, vol. 1, no. 1, 2014.

[51] X. Deng and E.A. Schiff, "Amorphous silicon based solar cells," in *Handbook of Photovoltaic Science and Engineering*, A. Luque and S. Hegedus, Eds. Chichester, UK: John Wiley & Sons, 2003, pp. 505–565.

[52] V. Manjunath, B.P. Reddy, U. Chalapathi, B. Son, H. Kim, C.H. Ahn, and S.H. Park, "Influence of single and double interlayers on the electrical and current transport mechanism of mo/n-si schottky diode and its microstructural and chemical properties," *Applied Physics A*, vol. 129, no. 7, p. 467, 2023.

[53] A.M. Bagher, M.M.A. Vahid, and M. Mohsen, "Types of solar cells and application," *American Journal of Optics and Photonics*, vol. 3, no. 5, pp. 94–113, 2015.

[54] TU Delft OpenCourseWare, "Solar energy – section 8.1: Semiconductor junctions," Delft University of Technology, n.d., retrieved May 24, 2025, from https://ocw.tudelft.nl/wp-content/uploads/solarenergysection81.pdf.

[55] A. Rogalski, *Infrared detectors*. Boca Raton, FL, USA: CRC Press, 2000.

[56] W. Yang, J. Chen, Y. Zhang, Y. Zhang, J.H. He, and X. Fang, "Silicon-compatible photodetectors: trends to monolithically integrate photosensors with chip technology," *Advanced Functional Materials*, vol. 29, no. 18, p. 1808182, 2019.

[57] Z. Wu, Y. Zhai, H. Kim, J.D. Azoulay, and T.N. Ng, "Emerging design and characterization guidelines for polymer-based infrared photodetectors,"

Accounts of Chemical Research, vol. 51, no. 12, pp. 3144–3153, 2018.

[58] F. Scholze, H. Rabus, and G. Ulm, "Mean energy required to produce an electron-hole pair in silicon for photons of energies between 50 and 1500 ev," *Journal of Applied Physics*, vol. 84, no. 5, pp. 2926–2939, 1998.

[59] S. Duttagupta, F. Ma, B. Hoex, T. Mueller, and A.G. Aberle, "Optimised antireflection coatings using silicon nitride on textured silicon surfaces based on measurements and multidimensional modelling," *Energy Procedia*, vol. 15, pp. 78–83, 2012.

[60] M. Casalino, G. Coppola, M. Iodice, I. Rendina, and L. Sirleto, "Near-infrared sub-bandgap all-silicon photodetectors: state of the art and perspectives," *Sensors*, vol. 10, no. 12, pp. 10 571–10 600, 2010.

[61] L. Fraas, "Solar cells, single-crystal semiconductors, and high efficiency," in *Solar Cells and Their Applications*, 2010, pp. 43–66.

[62] Stanford University, "Lecture notes on silicon photodetectors," n.d., retrieved May 24, 2025, from https://isl.stanford.edu/ abbas/ee392b/lect01.pdf.

[63] SPIE Digital Library, "Absorption efficiency enhancement of silicon photodetectors via nanophotonic photon management," 2024, https://www.spiedigitallibrary.org/conference-proceedings-of-spie/12991/129911O/...

[64] K. He, J.H. Cho, Y. Jung, S.T. Picraux, and J. Cumings, "Silicon nanowires: electron holography studies of doped p–n junctions and biased schottky barriers," *Nanotechnology*, vol. 24, no. 11, p. 115703, 2013.

[65] L. Chen, J.T. Ren, and Z.Y. Yuan, "Enabling internal electric fields to enhance energy and environmental catalysis," *Advanced Energy Materials*, vol. 13, no. 11, p. 2203720, 2023.

[66] B.E. Saleh and M.C. Teich, *Fundamentals of photonics*. New York: Wiley, 2008, vol. 332.

[67] Y. Fang and J. Huang, "Resolving weak light of sub-picowatt per square centimeter by hybrid perovskite photodetectors enabled by noise reduction," *Advanced Materials*, vol. 27, no. 17, pp. 2804–2810, 2015.

[68] A.G. Aberle, "Surface passivation of crystalline silicon solar cells: a review," *Progress in Photovoltaics: Research and Applications*, vol. 8, no. 5, pp. 473–487, 2000.

[69] B. Ceccaroli, E. Ovrelid, and S. Pizzini, *Solar silicon processes: Technologies, challenges, and opportunities*. Boca Raton, FL, USA: CRC Press, 2016.

[70] H. Gebrehiwet, "Absorption coefficient and dielectric function of direct band gap silicon nanocrystallites," Master's thesis, Addis Ababa University, Addis Ababa, Ethiopia, July 2007.

[71] L.C. Andreani, A. Bozzola, P. Kowalczewski, M. Liscidini, and L. Redorici, "Silicon solar cells: toward the efficiency limits," *Advances in Physics: X*, vol. 4, no. 1, p. 1548305, 2019.

[72] C. Ballif, F.J. Haug, M. Boccard, P.J. Verlinden, and G. Hahn, "Status and perspectives of crystalline silicon photovoltaics in research and industry," *Nature Reviews Materials*, vol. 7, no. 8, pp. 597–616, 2022.

[73] C. Battaglia, A. Cuevas, and S. De Wolf, "High-efficiency crystalline silicon solar cells: status and perspectives," *Energy & Environmental Science*, vol. 9, no. 5, pp. 1552–1576, 2016.

[74] J. Zhao, A. Wang, and M.A. Green, "24.5% efficiency silicon pert cells on mcz substrates and 24.7% efficiency perl cells on fz substrates," *Progress in Photovoltaics: Research and Applications*, vol. 7, no. 6, pp. 471–474, 1999.

[75] M. Tucci, L. Serenelli, S. de Iuliis, D. Caputo, and G. de Cesare, "Light trapping in thin silicon solar cells," in *Silicon Based Thin Film Solar Cells*, 2013, p. 395.

[76] H. Farrokhi, "Investigation into surface texturing by magnetic field assisted laser-produced plasma," Ph.D. dissertation, Nanyang Technological University, Singapore, 2013.

[77] F. Es, "Novel metal assisted etching technique for enhanced light management in black crystalline si solar cells," Doctoral dissertation, Middle East Technical University (Turkey), 2016.

[78] P. Singh, S.K. Srivastava, B. Sivaiah, P. Prathap, and C.M.S. Rauthan, "Enhanced photovoltaic performance of pedot: Pss/si solar cells using hierarchical light trapping scheme," *Solar Energy*, vol. 170, pp. 221–233, 2018.

[79] C. Huo, J. Wang, H. Fu, and K.Q. Peng, "Metal-assisted chemical etching of silicon: Origin, mechanism, and black silicon solar cell applications," in *Photovoltaic Manufacturing: Etching, Texturing, and Cleaning*, 2021, pp. 1–41.

[80] M. Mazur, D. Wojcieszak, J. Domaradzki, D. Kaczmarek, S. Song, and

F. Placido, "Tio2/sio2 multilayer as an antireflective and protective coating deposited by microwave assisted magnetron sputtering," *Opto-Electronics Review*, vol. 21, no. 2, pp. 233–238, 2013.

[81] M. Jabeen and S. Haxha, "High rear reflectance and light trapping in textured graphene based silicon thin film solar cells with back dielectric-metal reflectors," *OSA Continuum*, vol. 2, no. 5, pp. 1807–1821, 2019.

[82] I. Abdulhalim, "Coupling configurations between extended surface electromagnetic waves and localized surface plasmons for ultrahigh field enhancement," *Nanophotonics*, vol. 7, no. 12, pp. 1891–1916, 2018.

[83] P. Spinelli, V.E. Ferry, J. Van de Groep, M. Van Lare, M.A. Verschuuren, R.E.I. Schropp, and A. Polman, "Plasmonic light trapping in thin-film si solar cells," *Journal of Optics*, vol. 14, no. 2, p. 024002, 2012.

[84] E.S. Arinze, B. Qiu, G. Nyirjesy, and S.M. Thon, "Plasmonic nanoparticle enhancement of solution-processed solar cells: practical limits and opportunities," *ACS Photonics*, vol. 3, no. 2, pp. 158–173, 2016.

[85] H.A. Atwater and A. Polman, "Plasmonics for improved photovoltaic devices," *Nature Materials*, vol. 9, no. 3, pp. 205–213, 2010.

[86] A. Rudenko, J.P. Colombier, S. Höhm, A. Rosenfeld, J. Krüger, J. Bonse, and T.E. Itina, "Spontaneous periodic ordering on the surface and in the bulk of dielectrics irradiated by ultrafast laser: a shared electromagnetic origin," *Scientific Reports*, vol. 7, no. 1, p. 12306, 2017.

[87] A. Poruba, A. Fejfar, Z. Remeš, J. Špringer, M. Vaněček, J. Kočka, and A. Shah, "Optical absorption and light scattering in microcrystalline silicon thin films and solar cells," *Journal of Applied Physics*, vol. 88, no. 1, pp. 148–160, 2000.

[88] X. Li, Z. Gao, D. Zhang, K. Tao, R. Jia, S. Jiang, and X. Liu, "High-efficiency multi-crystalline black silicon solar cells achieved by additive assisted ag-mace," *Solar Energy*, vol. 195, pp. 176–184, 2020.

[89] J. Bonse *et al.*, "Laser-induced periodic surface structures—a scientific evergreen," *IEEE Journal of Selected Topics in Quantum Electronics*, 2017.

[90] H. Han, Z. Huang, and W. Lee, "Metal-assisted chemical etching of silicon and nanotechnology applications," *Nano Today*, vol. 9, no. 3, pp. 271–304, 2014.

[91] A.A. Leonardi, M.J.L. Faro, and A. Irrera, "Silicon nanowires synthesis by

metal-assisted chemical etching: A review," *Nanomaterials*, vol. 11, no. 2, p. 383, 2021.

[92] X. Li and P.W. Bohn, "Metal-assisted chemical etching in hf/h2o2 produces porous silicon," *Applied Physics Letters*, vol. 77, no. 16, pp. 2572–2574, 2000.

[93] J. Bonse, S.V. Kirner, and J. Krüger, "Laser-induced periodic surface structures (lipss)," in *Handbook of Laser Micro-and Nano-engineering*, K. Sugioka, Ed. Cham, Switzerland: Springer, 2020, pp. 1–59.

[94] X. Liu, P.R. Coxon, M. Peters, B. Hoex, J.M. Cole, and D.J. Fray, "Black silicon: fabrication methods, properties and solar energy applications," *Energy & Environmental Science*, vol. 7, no. 10, pp. 3223–3264, 2014.

[95] K. Nikolaidou, S. Sarang, and S. Ghosh, "Nanostructured photovoltaics," *Nano Futures*, vol. 3, no. 1, p. 012002, 2019.

[96] B.G. Rasheed and M.A. Ibrahem, "Laser micro/nano machining of silicon," *Micron*, vol. 140, p. 102958, 2021.

[97] L. Koker and K.W. Kolasinski, "Photoelectrochemical etching of si and porous si in aqueous hf," *Physical Chemistry Chemical Physics*, vol. 2, no. 2, pp. 277–281, 2000.

[98] M.L. Ngan, K.C. Lee, and K.W. Cheah, "Photochemical etching of silicon," *Journal of Porous Materials*, vol. 7, pp. 41–45, 2000.

[99] C. Edwards, K. Wang, R. Zhou, B. Bhaduri, G. Popescu, and L.L. Goddard, "Digital projection photochemical etching defines gray-scale features," *Optics Express*, vol. 21, no. 11, pp. 13 547–13 554, 2013.

[100] D. Dudley, W.M. Duncan, and J. Slaughter, "Emerging digital micromirror device (dmd) applications," in *MOEMS Display and Imaging Systems*, vol. 4985. SPIE, January 2003, pp. 14–25.

[101] A. Abdulkadir and M.Z. Pakhuruddin, "Effects of hydrogen peroxide concentration on properties of black silicon fabricated by two-step silver-assisted wet chemical etching for photovoltaics," *Iraqi Journal of Physics*, vol. 20, no. 2, pp. 11–25, 2022.

[102] Y. Liu, G. Ji, J. Wang, X. Liang, Z. Zuo, and Y. Shi, "Fabrication and photocatalytic properties of silicon nanowires by metal-assisted chemical etching: effect of h2o2 concentration," *Nanoscale Research Letters*, vol. 7,

pp. 1–9, 2012.

[103] V. Blattmann and D. Trusheim, "Hybrid laser-etching-process for wafer texturing," in *Energy Procedia*, vol. 77, 2015, pp. 766–773.

[104] S. Butkus, M. Rickus, R. Sirutkaitis, D. Paipulas, and V. Sirutkaitis, "Fabrication of high aspect ratio channels in fused silica using femtosecond pulses and chemical etching at different conditions," *Journal of Laser Micro Nanoengineering*, vol. 14, no. 1, pp. 19–24, 2019.

[105] C.C. Mai, "Thermal growth and chemical etching of silicon dioxide film," Master's thesis, Oregon State University, Corvallis, OR, USA, 1964.

[106] Z.T.M. Noori, "Efficiency response of a silicon solar cell to the photo-chemical etching process," *International Journal of Application or Innovation in Engineering & Management (IJAIEM)*, vol. 3, no. 4, pp. 74–80, April 2014.

[107] G. Fisher, M.R. Seacrist, and R.W. Standley, "Silicon crystal growth and wafer technologies," *Proceedings of the IEEE*, vol. 100, no. Special Centennial Issue, pp. 1454–1474, 2012.

[108] N. Roisin, G. Brunin, G.M. Rignanese, D. Flandre, and J.P. Raskin, "Indirect light absorption model for highly strained silicon infrared sensors," *Journal of Applied Physics*, vol. 130, no. 5, 2021.

[109] P. Campbell and M.A. Green, "Light trapping properties of pyramidally textured surfaces," *Journal of Applied Physics*, vol. 62, no. 1, pp. 243–249, 1987.

[110] M. Kovalev, I. Podlesnykh, A. Nastulyavichus, N. Stsepuro, I. Mushkarina, P. Platonov, and S. Kudryashov, "Efficient broadband light-trapping structures on thin-film silicon fabricated by laser, chemical and hybrid chemical/laser treatments," *Materials*, vol. 16, no. 6, p. 2350, 2023.

[111] R.E. Alsaigh, R. Bauer, and M.P. Lavery, "Multi-layer light trapping structures for enhanced solar collection," *Optics Express*, vol. 28, no. 21, pp. 31 714–31 728, 2020.

[112] A.K. Nath, "Laser etching and dry processing," *Bulletin of Materials Science*, vol. 11, pp. 159–166, 1988.

[113] M. Abbott and J. Cotter, "Optical and electrical properties of laser texturing for high-efficiency solar cells," *Progress in Photovoltaics: Research and Applications*, vol. 14, no. 3, pp. 225–235, 2006.

[114] A. Ibrahim and A.A. El-Amin, "Etching, evaporated contacts and antireflection coating on multicrystalline silicon solar cell," *International Journal of Renewable Energy Research*, vol. 2, no. 3, pp. 356–362, 2012.

[115] D.Y. Li, "Texturization of multicrystalline silicon solar cells," Ph.D. dissertation, Massachusetts Institute of Technology, Cambridge, MA, USA, 2010.

[116] A. Vinčiūnas, S. Indrišiūnas, B. Voisiat, G. Račiukaitis, I. Šimkienė, R. Suzanovičienė, and R. Mažeikienė, "Effect of laser patterning on properties of crystalline si photovoltaic cells and substrates," in *Laser*, vol. 200, 2013, p. 1030, nm.

[117] D.G. Coblas, A. Fatu, A. Maoui, and M. Hajjam, "Manufacturing textured surfaces: State of art and recent developments," *Proceedings of the Institution of Mechanical Engineers, Part J: Journal of Engineering Tribology*, vol. 229, no. 1, pp. 3–29, 2015.

[118] H.W. Sun, L. Li, L.J. Gu, J.S. Wang, L.X. Zhang, Y. Gu, and X.Y. Bao, "Nanoimprint lithography for solar cell applications," *Journal of Nanoelectronics and Optoelectronics*, vol. 19, no. 11, pp. 1075–1097, 2024.

[119] W. Lee and S.J. Park, "Porous anodic aluminum oxide: anodization and templated synthesis of functional nanostructures," *Chemical Reviews*, vol. 114, no. 15, pp. 7487–7556, 2014.

[120] M.L. Brongersma, Y. Cui, and S. Fan, "Light management for photovoltaics using high-index nanostructures," *Nature Materials*, vol. 13, no. 5, pp. 451–460, 2014.

[121] J. Zhu, Z. Yu, S. Fan, and Y. Cui, "Nanostructured photon management for high performance solar cells," *Materials Science and Engineering: R: Reports*, vol. 70, no. 3-6, pp. 330–340, 2010.

[122] A.P. Amalathas and M.M. Alkaisi, "Nanostructures for light trapping in thin film solar cells," *Micromachines*, vol. 10, no. 9, p. 619, 2019.

[123] M. Stafe, A. Marcu, and N.N. Puscas, "Material removal and deposition by pulsed laser ablation and associated phenomena," in *Pulsed Laser Ablation of Solids: Basics, Theory and Applications*, 2014, pp. 143–214.

[124] T. Fang, J. An, Q. Chen, Y. He, H. Wang, and X. Zhang, "Progress and comparison in nondestructive detection, imaging and recognition technology for defects of wafers, chips and solder joints," *Nondestructive Testing and Evaluation*, vol. 39, no. 6, pp. 1599–1654, 2024.

[125] I. Massiot, C. Trompoukis, K. Lodewijks, V. Depauw, and A. Dmitriev, "Highly conformal fabrication of nanopatterns on non-planar surfaces," *Nanoscale*, vol. 8, no. 22, pp. 11 461–11 466, 2016.

[126] M.A. Green, *Silicon solar cells: Advanced principles & practice*. Sydney, Australia: Centre for Photovoltaic Devices and Systems, University of New South Wales, 1995.

[127] M. Hermle, F. Feldmann, M. Bivour, J.C. Goldschmidt, and S.W. Glunz, "Passivating contacts and tandem concepts: Approaches for the highest silicon-based solar cell efficiencies," *Applied Physics Reviews*, vol. 7, no. 2, 2020.

[128] A. Cuevas and D. Macdonald, "Measuring and interpreting the lifetime of silicon wafers," *Solar Energy*, vol. 76, no. 1-3, pp. 255–262, 2004.

[129] R. Venkatesan, J. Mayandi, T.G. Finstad, J.M. Pearce, and V. Venkatachalapathy, "Nanostructured silicon for solar energy conversion applications," in *Nanomaterials for Energy and Sensor Applications*. CRC Press, 2024, pp. 54–93.

[130] S.E. Han and G. Chen, "Toward the lambertian limit of light trapping in thin nanostructured silicon solar cells," *Nano Letters*, vol. 10, no. 11, pp. 4692–4696, 2010.

[131] R. Brendel, *Thin-film crystalline silicon solar cells: Physics and technology*. Chichester, West Sussex, UK: John Wiley & Sons, 2011.

[132] M. Spence, R. Hammond, A. Pockett, Z. Wei, A. Johnson, T. Watson, and M.J. Carnie, "A comparison of different textured and non-textured anti-reflective coatings for planar monolithic silicon-perovskite tandem solar cells," *ACS Applied Energy Materials*, vol. 5, no. 5, pp. 5974–5982, 2022.

[133] H. Liu, M.H. Yu, C.C. Lee, X. Yu, Y. Li, Z. Zhu, and A.K.Y. Jen, "Technical challenges and perspectives for the commercialization of solution-processable solar cells," *Advanced Materials Technologies*, vol. 6, no. 6, 2021.

[134] Z. Fan, D. Cui, Z. Zhang, Z. Zhao, H. Chen, Y. Fan, and S. Yan, "Recent progress of black silicon: From fabrications to applications," *Nanomaterials*, vol. 11, no. 1, p. 41, 2020.

[135] J. Lv, T. Zhang, P. Zhang, Y. Zhao, and S. Li, "Review application of nanostructured black silicon," *Nanoscale Research Letters*, vol. 13, pp. 1–10, 2018.

[136] W. Qarony, M.I. Hossain, M.K. Hossain, M.J. Uddin, A. Haque, A.R. Saad, and Y.H. Tsang, "Efficient amorphous silicon solar cells: characterization, optimization, and optical loss analysis," *Results in Physics*, vol. 7, pp. 4287–4293, 2017.

[137] M.A. Green, "Solar cell fill factors: General graph and empirical expressions," *Solid-State Electronics*, vol. 24, no. 8, pp. 788–789, 1981.

[138] E.D. Palik, Ed., *Handbook of optical constants of solids*. San Diego, CA, USA: Academic Press, 1998, vol. 3.

[139] W. Shockley and H.J. Queisser, "Detailed balance limit of efficiency of p–n junction solar cells," in *Renewable Energy*. Routledge, 2018, pp. Vol2_35–Vol2_54.

[140] S. Kontermann, T. Gimpel, A.L. Baumann, K.M. Guenther, and W. Schade, "Laser processed black silicon for photovoltaic applications," in *Energy Procedia*, vol. 27, 2012, pp. 390–395.

[141] H. Savin, P. Repo, G. Von Gastrow, P. Ortega, E. Calle, M. Garín, and R. Alcubilla, "Black silicon solar cells with interdigitated back-contacts achieve 22.1% efficiency," *Nature Nanotechnology*, vol. 10, no. 7, pp. 624–628, 2015.

Appendix A

Zemax Optical Model Design

This appendix presents the optical design of the beam expander developed to achieve a laser beam diameter of 4 cm.

	Object Type	Comment	Ref Object	Inside Of	X Position	Y Position	Z Position	Tilt About X	Tilt About Y	Tilt About Z	Material	X Half Width	Y Half Width
1	Source Ellipse	Field 1	0	0	0.00000	0.00000	-22.86000	0.00000	0.00000	-180.000...		10	1E+06
2	Standard Lens	Beam Expander	0	0	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	N-BK7	21.78000	0.00000
3	Standard Lens	Collimator	0	0	0.00000	0.00000	112.60000	0.00000	0.00000	0.00000	N-BK7	-0.00000	0.00000
4	Null Object	Image Plane	3	0	0.00000	0.00000	200.00000	0.00000	0.00000	0.00000	-		
5	Detector Rectangle	Field 1	4	0	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000		25.00000	25.00000

Figure A.1 Zemax optical model parameters.

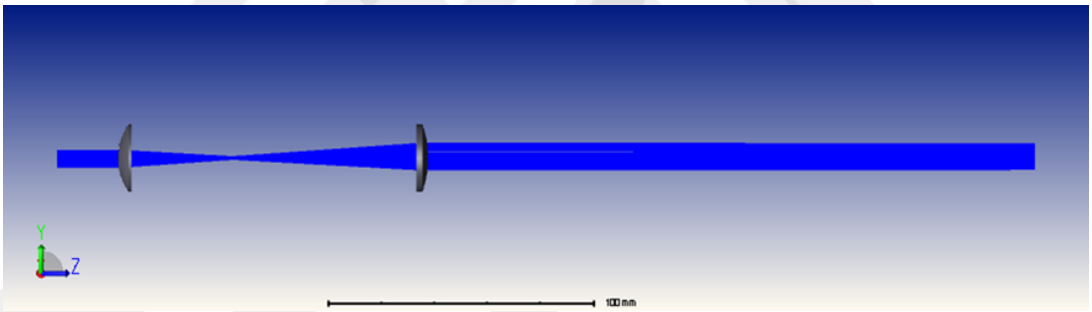


Figure A.2 Zemax optical model design layout.

Appendix B

Conference Contribution

This study was partially presented at the following international congress:

> **Güntuğ Vural**, Alpan Bek, Reşat Özgür Doruk. *Photochemical Laser Etching of Randomly Distributed Inverted Nanoholes on Crystalline Silicon*. **5th International Congress of Engineering and Natural Sciences (ICENSS 2025)**, May 24–25, 2025, Ankara, Türkiye. ISBN: 978-625-372-661-4. Pages 229–241.

The abstract of the published conference paper is reproduced below:

> While crystalline silicon solar cells currently dominate the photovoltaic market, improving their efficiency through advanced surface texturing remains a significant research challenge. This study introduces an innovative single-step inverted nanohole (SS-INH) surface texturing approach using in-situ photochemical etching (PCE) on n-type silicon solar cells, employing a continuous-wave laser (532 nm) in an HF/H_2O_2 aqueous solution. The nanostructures produced via PCE have been shown to be denser and more effective across a broad spectral range compared to conventional texturing techniques. Scanning electron microscopy (SEM) confirmed the uniformity of the inverted nanoholes. Photon trapping was significantly enhanced, as evidenced by reduced average reflectance, down to 17.5% for saw damaged (SD) and 22.5% for saw damage removed (SDR), along with increased haze resulting from enhanced light scattering. Comparative analyses between SD and SDR wafers highlighted the superior electrical characteristics of SDR surfaces, notably reduced defect-induced recombination. Furthermore, simultaneous photochemical

etching demonstrated distinct advantages over conventional sequential methods, including continuous oxide removal, and improved profile anisotropy suitable for MEMS fabrication. Notably, the proposed method (SS-INH-PCE) inherently eliminates the need for a separate SDR step, simplifying the process and reducing overall chemical and thermal loads. The simplicity, reproducibility, and optical efficiency of the process highlight its potential for scalable industrial integration, positioning inverted nanohole texturing as a promising pathway for next-generation high-efficiency solar cells and MEMS technologies.

The full text of the paper is available in the official proceedings of the ICENSS 2025 conference.